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GUEST EDITORIAL

Special Section Guest Editorial: Patterning for Advanced Packaging

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More-than-Moore approaches to improving system performance have been a hot topic for a decade. Advanced packaging is a key contributor in more-than-Moore approaches. It realizes a chiplet approach with wide-band interconnection among SoCs and memories for high-performance computing.

The different patterning technologies from one for front-end-of-line (FEOL) are required in advanced packaging. Examples of such technologies include vertical profile in thick resist, large exposure field, warped substrate handling, specific EDA design rule, etc.

One of the big discussions in advanced packaging is whether to adopt a wafer-level packaging or panel-level packaging substrate platform. Wafer-level packaging is the expansion of FEOL processes, and it has advantages of finer patterning, higher yield, and higher reliability. On the other hand, panel-level packaging is an advancement of build-up substrate processes, and it has advantages on cost and larger package size. In particular, the cost advantage of panel-level package increases in larger packages more than 50 mm square because the effective area of the wafer-level package rapidly decreases in larger packages.

This Special Section on Patterning for Advanced Packaging has papers from both the viewpoint of the wafer-level packaging patterning tools manufacturer and the panel-level packaging tools manufacturer. The editors believe that readers can enjoy comparing each advantage and challenge.

The paper by Bravo et al. discusses EDA technology to reduce cracks during the dicing process. Since cutting-edge chips become thinner and thinner, the barrier proposed in the paper will help improve yield and reliability.

The paper by Shinoda et al. discusses a wafer-level packaging patterning tool. Their tool started from a FEOL tool, and they report low distortion advantage for fine pitch bump patterning.

The paper by Sohara et al. discusses a panel-level packaging patterning tool. Their tool is a fine build-up substrate patterning tool, and it has wide 250 mm square exposure that is suitable for next-generation advanced panel-level packaging.

The last paper by Suda et al. discusses a unique panel level stepper. It equips FEOL technologies and panel handling system. It may extend the resolution limit of panel-level packaging.

We hope this special section will provide JM^3 readers with an introduction to and review of this exciting part of the field of semiconductor lithography. We know there is a great deal of exciting work in resist processing, direct write lithography, metrology, and other topics of relevance to our readers, and we encourage other researchers in the AP field to submit their work to future issues of JM^3. We thank the authors, reviewers, and the JM^3 staff for their contributions.