Metrology

This special section on metrology explores new developments, issues, and solutions for both reticle- and wafer-level metrology. Much of the attention of semiconductor lithographers is devoted to exposure tools and process. However, as feature sizes and process tolerances shrink, the requirements for metrology speed, precision, long-term stability, matching, process robustness, and total measurement uncertainty shrink as well. Current critical dimension (CD) and overlay metrology requirements for the 32-nm node and below are well below the size of a single silicon atom (0.25 nm). This creates an increasingly challenging environment for lithographic metrologists and drives the need both to improve existing metrology techniques as well as to develop new metrology technologies. Additional metrology challenges include the lack of calibrated standards for both CD and overlay; the need for increasing volumes of data to meet evolving process control requirements; and new metrology requirements imposed by double patterning, complex three-dimensional structures (vertical scaling), and other new forms of device scaling that drive the need for unique new measurements.

We appreciate the work of the authors and reviewers who have contributed to this special section, and we hope the JM^3 readership will find this collection of papers valuable.

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