SILICON WAFER-BASED TANDEM CELLS: THE ULTIMATE PHOTOVOLTAIC SOLUTION?

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ABSTRACT

Recent large price reductions with wafer-based cells have increased the difficulty of dislodging silicon solar cell technology from its dominant market position. With market leaders expected to be manufacturing modules above 16% efficiency at $0.36/Watt by 2017, even the cost per unit area ($60-$70/m^2) will be difficult for any thin-film photovoltaic technology to significantly undercut. This may make dislodgement likely only by appreciably higher energy conversion efficiency approaches. A silicon wafer-based cell able to capitalize on on-going cost reductions within the mainstream industry, but with an appreciably higher than present efficiency, might therefore provide the ultimate PV solution. With average selling prices of 156 mm quasi-square monocrystalline Si photovoltaic wafers recently approaching $1 (per wafer), wafers now provide clean, low cost templates for overgrowth of thin, wider bandgap high performance cells, nearly doubling silicon's ultimate efficiency potential. The range of Si-based tandem approaches is reviewed together with recent results and ultimate prospects.

Keywords: Silicon Solar Cells, Tandem, High-Efficiency

1. INTRODUCTION

Figure 1 shows that using high quality, inexpensive silicon wafers as templates for the growth of overlying high performance cells offers limiting efficiency close to the maximum possible. I fthe costs of doing this can be kept small compared to relatively fixed module costs such as those of module encapsulation, frames and junction boxes, this offers the potential for a higher efficiency product at lower cost per unit power or energy output. A range of techniques for producing such tandem cell stacks currently under investigation both within the authors' groups and elsewhere are outlined and recent progress is reviewed. Key contenders include both GaP/GaAs and Si/Ge metamorphic approaches, "monolayer" interfacial strain relaxation approaches, lattice matched approaches using III-V alloys, chalcogenides or strain-balanced, short-period superlattices, "all-silicon" tandems based on manipulating silicon's bandgap using quantum confinement, new materials such as perovskites; or finally, mechanically stacking exfoliated cells on a silicon wafer.

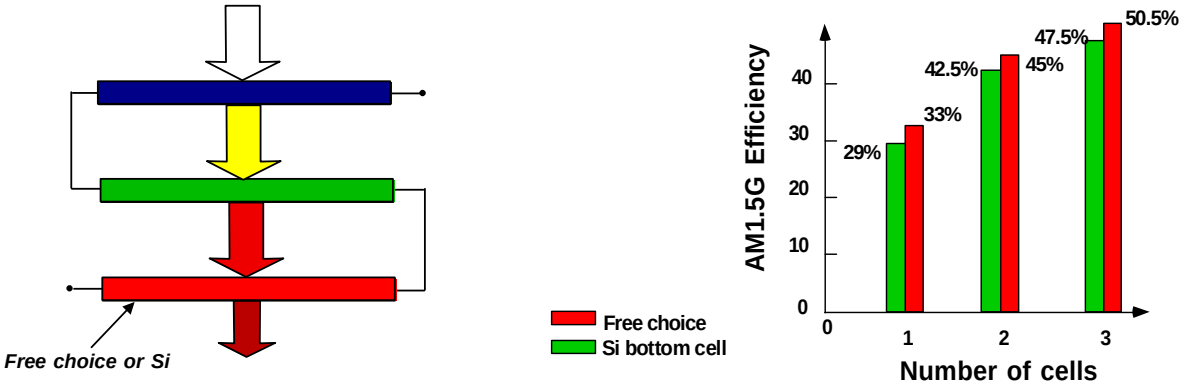

Figure1. Tandem cell stack and limiting efficiency, with (green) and without (red) the bottom cell constrained to be silicon.

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2. WAFER PRICES/DEPOSITION COSTS

Average selling prices (ASP) of monocrystalline 156 mm quasi-square silicon wafers for photovoltaic use have reduced from a high of $10/wafer in 2008 to just over $1/wafer at the end of 2012 (Fig. 2a). Similarly low prices prevailed during 2013.

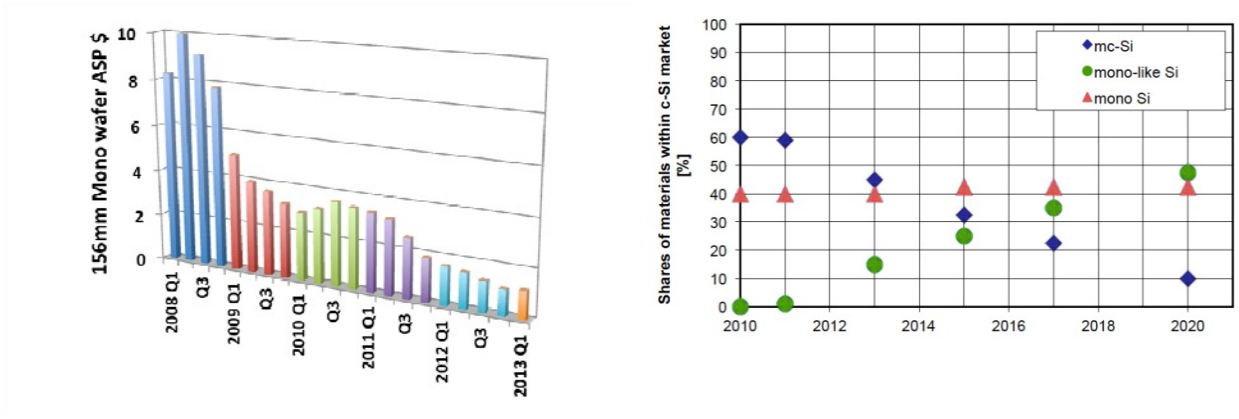


Figure 2. (a) Quarterly ASP of mono 156 nm quasi-square Si wafers 2008-2013 (various sources); (b) International Technology Road Map (ITRPV) market share projections of mono and mono-like wafers (March 2012).

Ongoing price reductions are anticipated from reduced crystallisation costs, including the production of "quasi-mono" material, and from improved sawing processes as well as from thinner wafers. The 2012 ITRPV Roadmap (Fig. 2b) shows what might be possible, particularly given an additional incentive such as provided by the present work, with 90% of all wafers used by the industry projected to be mono or mono-like by 2020. These inexpensive, high-quality wafers would provide ideal templates for the overgrowth of thin, crystalline, wider-bandgap cells, greatly boosting the efficiency potential of Si wafer-based approaches. Even if multicrystalline materials remain the norm, some approaches, such as those involving perovskites would work well.

MOCVD deposition costs for III-V materials are presently high but large reductions are expected due to the expensive growth of the LED lighting market. Costing studies for photovoltaic use suggests competitive costs could ultimately be attained [1]. The closest step in present silicon cell processing is PECVD deposition of a circa 70 nm nitride antireflection coating, costing less than 5c/W to deposit [1].

3. EFFICIENCY GAINS

Figure 1 shows the limiting efficiency of tandem cell stacks on Si compared to that of stacks with a free choice of substrate. All cells are assumed to be radiatively limited, apart from the Si cell where performance is limited by intrinsic Auger recombination. For a 2-cell stack, the optimum bandgap of the top cell is 1.7 eV, although a lower bandgap cell can be used if partly transmissive of wavelengths above its bandgap. For a 3-cell stack, the optimal bandgaps for the upper cells are 2.0 eV and 1.5 eV, although again lower values can be used if these cells are partly transmissive. Such partly transmissive designs may be preferred in practice since they will reduce the thickness of deposited material required. Increasing the number of cells in the stack continues to increase Si-based cell efficiency, but at a slower rate than for the unconstrained case.

The highest efficiency tandem cells to date use GaInP/Ga(In)As as the two uppermost cells (and either GaInAs or Ge as the bottommost cell), with efficiencies in the 35-40% range for 3-cell stacks for non-concentrated sunlight. Using these two uppermost cells on a Si substrate is likely to give the quickest path to high efficiency both in a monolithic or a mechanical stack, although a range of other options may be able to be developed to a similar level of sophistication in the future.

4. OPTIONS

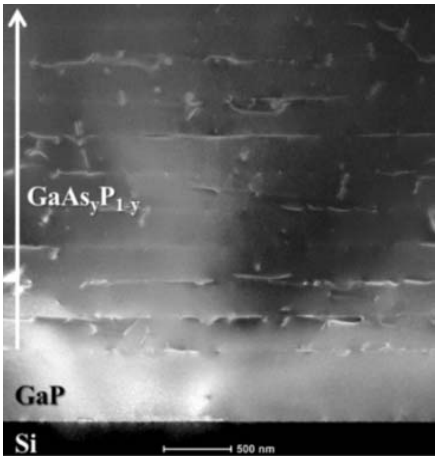
Key options include both GaP/GaAs and Si/Ge metamorphic approaches, "monolayer" interfacial strain relaxation approaches, lattice matched approaches using III-V alloys, chalcogenides or strain-balanced, short-period superlattices, "all-silicon" tandems based on manipulating silicon's bandgap using quantum confinement, new materials such as perovskites; or finally, mechanically stacking exfoliated cells on a silicon wafer.

4.1 Metamorphic approaches

Coolaborators at the Ohio State University have pioneered the growth of III-V cells on silicon for solar applications [2-4] through metamorphic structures based on graded $GaAs_yP_{1-y}$ or Ge_ySi_{1-y} buffer layers (Fig. 3a). Of these approaches, the former is preferred on device grounds, since the $GaAs_yP_{1-y}$ bandgap is higher than that of Si allowing the Si substrate to be used as an active cell in he stack. The buffer layer can serve as a heteroface window for the Si cell as well as accommodating the tunnelling/defect junction required to connect overlying cells in series with the Si cell.

Good preliminary results have been obtained in interfacing the underlying Si cell with overlying layers (Fig. 3b). This is the most likely route to demonstration of a near-term efficiency above 30% in a monolithic tandem device on silicon. One disadvantage is the deposition time required for the buffer layer, which may be as thick as or thicker than the overlying cells (Fig. 3a).

(a)



(b)

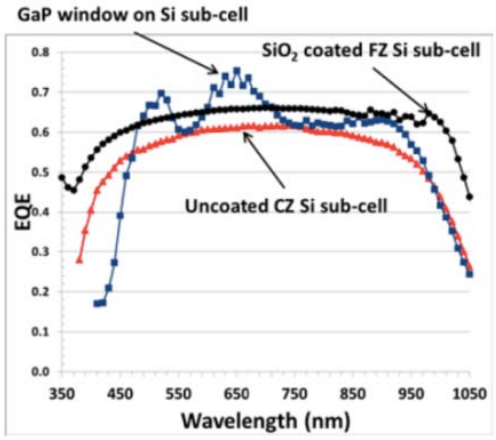


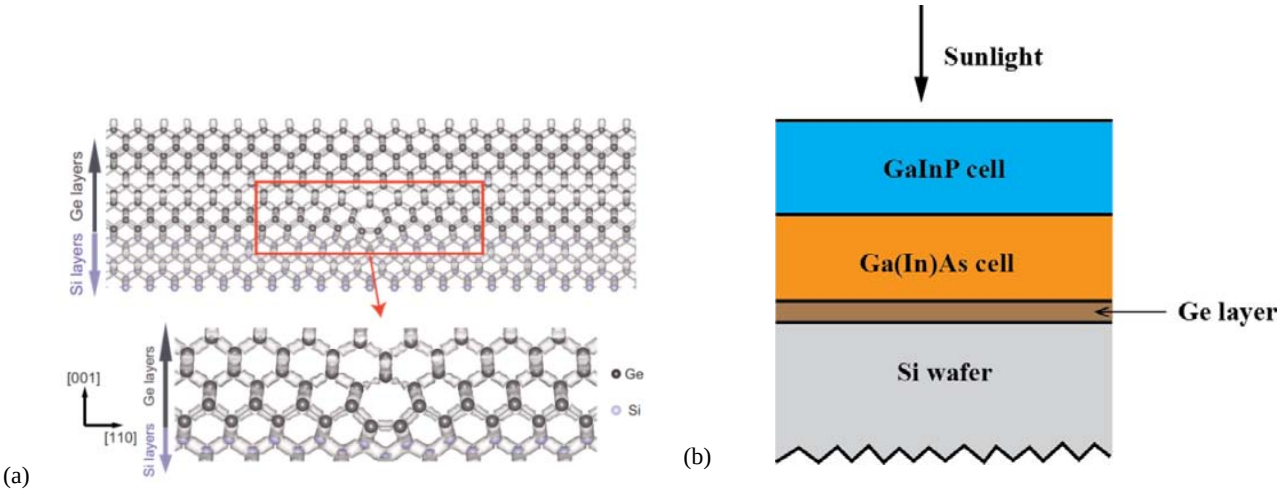
Figure 3. (a) Cross-sectional dark-field STEM image of an MOCVD GaAs0.7 P0.3/ step graded GaAsyP1-y/Si structure [2]; (b) EQE for CZ Si sub-cells with and without a GaP epitaxial front window. Also shown is the improved infrared response of a FZ Si bottom layer cell developed for this work [2].

4.2 "Monolayer" interfacial strain relaxation

Analysis of the energetics of the Ge/Si interface [5] shows that after the deposition of 12 Ge atomic layers, the lowest energy configuration switches from a strained Ge layer lattice lattice-matched to Si to a relaxed structure with 90^o dislocations parallel to the interface. Experimentally this configuration is rarely seen. Rather, high densities of threading dislocations propagate through the Ge film to overlying layers. This is generally attributed to the tendency for growth to occur via the islanded Stranski-Krastanov (SK) mechanism [5]. The buffer layer structures as above are then required to subdue these threading dislocations. Avoiding threading dislocations has obvious advantages with recent work suggesting this is possible using surfactants to encourage monolayer by monolayer rather than SK growth [4].

UNSW is working on approaches to producing very thin relaxed Ge layers on Si which would then provide a "virtual Ge" substrate for the subsequent deposition of high performance III-V cells. If the Ge layer is sufficiently thin (<50 nm), an "out-of-sequence" tandem cell becomes possible. Light-trapping applied to the rear of the Si cell either by texturing or

plasmonic scattering would also increase the effectiveness of such a thin Ge layer in absorbing light below the Si bandgap. This provides possibly the second most likely route to near-term monolithic device implementation.



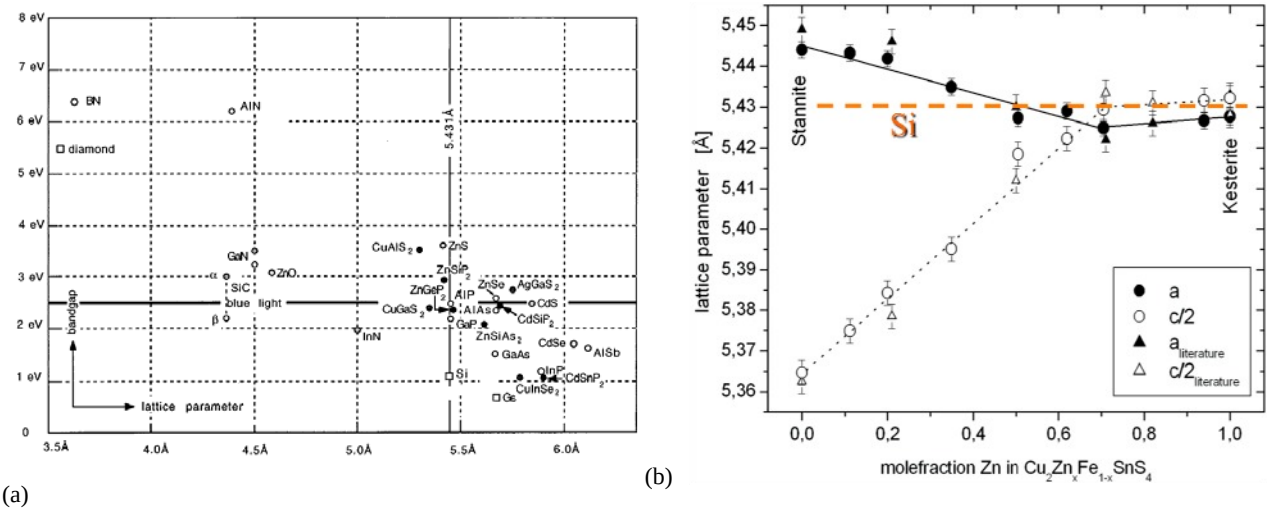
(a) (b)

Figure 4. (a) "Lattice matching in a monolayer" – lowest energy configuration for Ge on Si, once more than 12 monolayers deposited (after [3]); (b) "Out-of-sequence" tandem. Photons are shared between the Si and Ge, with rear light-trapping features increasing Ge absorption of photons below the Si bandgap.

4.3 Lattice matched approaches

4.3.1 III-V cells

From Fig. 5a, GaN and AIN have smaller lattice spacing than Si, allowing alloys with phosphides and arsenides to be lattice matched. The properties of the alloy system $GaN_xP_{1-x-y}As_y$ has been investigated in some detail [7]. Alloys with bandgaps in the range 1.5-2.0 have been synthesized [7] with operational monolithic cell on Si demonstrated [7]. Performance has been modest due to the less than ideal properties of layers incorporating substantial N. If this issue could be solved, a triple junction stack within this material system would be possible.



(a) (b)

Figure 5. (a) Bandgap versus lattice parameter of a range of semiconductor compounds [6]; (b) Lattice match to kesterite and stannite.

4.3.2 Chalcogenide cells

As apparent from Fig. 5, some chalcogenide compounds are close to being lattice-matched to Si. Of particular interest is CZTS (kesterite), with both it and alloys with stannite (Cu_2FeSnS_4) being in this class (Fig. 5b). The advantage of this material system is that it is likely to attract significant research attention over the coming decade as a non-toxic, earth-abundant alternative to both CdTe and CIGS thin-films. Thin-film tandem cells in this system are also likely to be of increasing interest, given the likely need for any alternative to Si to at least match its energy conversion efficiency. The present work could build on such developments. The first step is to demonstrate CZTS epitaxy on Si, with this being recently achieved at NREL and on sapphire at UNSW.

4.3.3 Strain balanced layers

Another approach to lattice matching is to use strain-balanced layers as has proved effective in III-V cell technology [10]. Strain balancing of $GaN_xP_{1-x-y}As_y$ layers has also been explored [11], given the superior properties of the dilute nitrides. More radical combinations may be possible, as suggested by Fig. 5a, if thicknesses are restrained to a few monolayers. Layer by layer deposition approaches may be particularly attractive to allow the required control and may be economically feasible for semitransparent layers with wavelength selective light-trapping features, as developed for "micromorph" cells.

4.4 Amorphous or perovskite layers

Amorphous upper cells would remove the need for lattice matching, with the micromorph cell an example of this. Other possibilities would be Si quantum dots in an amorphous matrix, as explored in earlier UNSW work [12]. The challenge here is in getting sufficiently good performance from these cells, since this must be better than that from the Si substrate.

A recent development relevant to this general approach has been the emergence of perovskite solar cells [13,14,15]. These have already demonstrated confirmed efficiencies of over 14% when deposited by simple approaches onto non-crystalline substrates. Key features are a high open-circuit voltage relative to the bandgap (~1.6 eV) and the potential for near term efficiency gains. Simulations show that deposition of a single perovskite cell of even the present quality on the best quality PERL c-Si cells has the potential to increase efficiency from 25% to above 27%, with improvements becoming larger for poorer quality c-Si cells and substrates. Efficiency above 22% appears feasible, for example, if a perovskite cell is stacked on a normal multicrystalline screen-printed cell and above 20% if stacked on low grade multicrystalline Si cells, such as might be fabricated from upgraded metallurgical grade silicon. The expected ongoing improvements in perovskite cell performance will correspondingly increase tandem cell performance. Perovskites based on $Ch_3NH_3PbI_3$ and the higher bandgap $CH_3NH_3PbBr_3$, $CH_3NH_3PbCl_3$ and their alloys look interesting for 2 and 3 cell stacks. On the downside, there are presently questions about perovskite cell stability and also the high weight percentage of Pb in present implementations is certain to raise environmental concerns.

4.5 Mechanical stacks

Another approach that overcomes problems with lattice mismatch is mechanical stacking. Stacking a thin GaAs cell on a Si cell produced 30% efficiency under concentration back in 1988, using an exfoliated GaAs cell produced by the Kopin Corporation using the CLEFT process. Recent work by Alta Devices has led to improved performance for exfoliated GaAs devices to 29.1% efficiency and 30.8% efficiency of GaInP/GaAs dual junction devices. Stacking such a device on Si with design changes to make the top cells transparent to sub-bandgap wavelengths would result in an efficiency boost without adding significantly to costs.

5. DISCUSSION AND CONCLUSION

The above approaches can be compared using a matrix of key indicators, including probability of successful medium term implementation, likely performance, thermal expansion issues and likely cost.

The III-V approaches offer the ultimate in efficiency from the Si tandem approach and realistic opprotunities for near-term implementation. The III-V based tandems may be ideal for applications such as concentrator cells where cost constraints can be relaxed.

CZTS-based cells offer the opportunity for lattice matching to Si with potentially low costs. There is considerably more uncertainty, however, regarding the timescale for implementation of high performance devices.

Perovskite-silicon tandem cells look particularly interesting for near-term implementatin at low cost. Issues in this case relate to the poorer stability of the perovskite cells compared to silicon and the high percentages of toxic Pb in the most successful implementations to date.

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