

PROCEEDINGS OF SPIE

Design-Process-Technology Co-optimization XV

Chi-Min Yuan
Ryoung-Han Kim
Editors

22–26 February 2021
Online Only, United States

Sponsored by
SPIE

Cosponsored by
Hitachi High Technologies, America, Inc. (United States)

Published by
SPIE

Volume 11614

Proceedings of SPIE 0277-786X, V. 11614

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

Design-Process-Technology Co-optimization XV, edited by Chi-Min Yuan, Proc. of SPIE Vol. 11614,
1161401 · © 2021 SPIE · CCC code: 0277-786X/21/\$21 · doi: 10.1117/12.2595827

Proc. of SPIE Vol. 11614 1161401-1

The papers in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. Additional papers and presentation recordings may be available online in the SPIE Digital Library at SPIDigitalLibrary.org.

The papers reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from these proceedings:

Author(s), "Title of Paper," in *Design-Process-Technology Co-optimization XV*, edited by Chi-Min Yuan, Ryoung-Han Kim, Proceedings of SPIE Vol. 11614 (SPIE, Bellingham, WA, 2021) Seven-digit Article CID Number.

ISSN: 0277-786X
ISSN: 1996-756X (electronic)

ISBN: 9781510640610
ISBN: 9781510640627 (electronic)

Published by

SPIE

P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445

SPIE.org

Copyright © 2021, Society of Photo-Optical Instrumentation Engineers.

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is \$21.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/21/\$21.00.

Printed in the United States of America by Curran Associates, Inc., under license from SPIE.

Publication of record for individual papers is online in the SPIE Digital Library.

**SPIE. DIGITAL
LIBRARY**

SPIDigitalLibrary.org

Paper Numbering: *Proceedings of SPIE* follow an e-First publication model. A unique citation identifier (CID) number is assigned to each article at the time of publication. Utilization of CIDs allows articles to be fully citable as soon as they are published online, and connects the same identifier to all online and print versions of the publication. SPIE uses a seven-digit CID article numbering system structured as follows:

- The first five digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B ... 0Z, followed by 10-1Z, 20-2Z, etc. The CID Number appears on each page of the manuscript.

Contents

DESIGN FOR RELIABILITY: TECHNOLOGY, IP AND SYSTEM

- 11614 03 **Design-technology co-optimization for reliability and quality in advanced nodes (Invited Paper)** [11614-1]

PATTERN-BASED DESIGN OPTIMIZATION

- 11614 06 **Pattern-centric yield management approach with machine learning to detect and track defects with full chip coverage** [11614-4]
- 11614 08 **Rule-based hotspot correction using a pattern matching flow** [11614-6]
- 11614 09 **Pattern similarity profiling using semi-supervised learning algorithm** [11614-7]
- 11614 0A **A quantified approach of dataset selection for training ML models on hard-to-classify patterns** [11614-8]

DTCO FOR STANDARD CELLS AND MEMORY

- 11614 0E **SSVT (six stacked vertical transistors) SRAM cell architecture introduction: design and process challenges assessment** [11614-12]
- 11614 0G **Extending materials to systems co-optimization™ (MSCO™) modeling to memory array simulation** [11614-14]

DTCO FOR DEVICE AND INTEGRATION

- 11614 0H **Fine-pitch 3D system integration and advanced CMOS nodes: technology and system design perspective (Invited Paper)** [11614-15]
- 11614 0I **Scatterometry-based calibration of a 3D virtual fabrication model for gate-all-around devices** [11614-16]
- 11614 0J **Reducing stress effects on multi-project-wafer reticles by optimizing metal densities and density gradients in an MPW placement flow** [11614-17]
- 11614 0L **Electrical design-for-manufacturability (DFM) checks for reducing layout-induced circuit variability of analog designs** [11614-19]

MACHINE LEARNING ON OPC

- 11614 0M **Fast 3D lithography simulation by convolutional neural network** [11614-21]
- 11614 0O **Machine learning based recursive partitioning for simplifying OPC model building complexity**
[11614-23]
- 11614 0P **Source mask optimization based on design pattern library at 7nm technology node** [11614-24]
- 11614 0Q **EUV single patterning exploration for pitch 28 nm** [11614-25]

DTCO BY EDA VENDORS

- 11614 0S **Ab initio for design-technology co-optimization (Invited Paper)** [11614-27]
- 11614 0T **Applying machine learning methods to accelerate advanced process node yield ramp**
(Invited Paper) [11614-28]

MACHINE LEARNING ON HOTSPOT DETECTION

- 11614 0V **Machine-learning assisted fast critical area analysis** [11614-30]
- 11614 0W **Multi-level layout hotspot detection based on multi-classification with deep learning** [11614-31]
- 11614 0X **Deep learning-based hotspot prediction of via printability in process window corners** [11614-32]
- 11614 0Y **Guard-banding of IP against topography sensitivity using silicon-calibrated CMP model**
[11614-34]

DTCO BY EQUIPMENT VENDORS

- 11614 10 **Analysis of row to row routing in double height standard-cells (Invited Paper)** [11614-36]

POSTER SESSION

- 11614 13 **Fast, high-capacity critical area analysis (CAA) with advanced FINFET defectivity calculation**
[11614-39]