Image acquisition module based on FPGA

Xiaoming Chen[a], Chinta Chen[a*], Fengchia Chuang[b], Chaobin Chen[a], Huan Ma[a], Xuxin Cheng[a]
[a]Electronic and Electrical Engineering, Zhaoqing University, Zhaoqing 526000, Guangdong, China;
[b]College of Mechanical and Automotive Engineering, Zhaoqing University, Zhaoqing 526000, Guangdong, China

ABSTRACT

This paper proposes an image acquisition module based on Field Programmable Gate Array (FPGA), aiming to realize image acquisition and processing. This module design mainly uses ADV7180 chip, camera OV5640, and synchronous dynamic random access memory (SDRAM) memory. This module includes functional modules such as image sensor interface, data cache, image processing, and image storage, and uses the parallel computing power of FPGA to implement image acquisition processing tasks. FPGA-based modules have significant advantages in image acquisition and processing through their parallel computing capabilities and reconfigurability. Then the design and implementation of the FPGA-based image acquisition module offers higher processing speed and lower latency than traditional software implementations.

Keywords: FPGA, image acquisition module, image processing

1. INTRODUCTION

With the continuous advancement of science and technology, digital image processing plays a key role in many fields, such as medical imaging, industrial testing, security monitoring, etc. To achieve high-quality image acquisition and real-time processing, researchers are constantly looking for efficient, flexible, and reconfigurable platforms. Image acquisition modules based on field programmable gate array (FPGA) have attracted much attention due to their parallel computing capabilities and flexibility[1].

Field programmable gate array (FPGA) is a logic programming software with a high degree of parallel processing capabilities and flexible hardware reconfiguration. Compared with traditional general-purpose processors, it can perform multiple tasks in parallel and process large amounts of data in real time. Therefore, it is a good choice for image processing and high-performance computing[2].

In the field of image acquisition, FPGA can be used to build high-performance image acquisition modules and realize real-time image processing tasks through its parallel computing capabilities[3]. FPGA can be used as an interface to an image sensor to collect and process data output by the sensor in real time. In addition, it can also implement image preprocessing functions, such as denoising, enhancement, geometric correction, etc., to improve image quality.

As the demand for high-definition and high-frame-rate images continues to increase, traditional software implementations may not be able to meet the real-time and computational complexity requirements. The FPGA-based image acquisition module can solve these challenges through hardware acceleration and parallel processing, providing higher performance and efficiency.

In addition, the reconfigurable nature of FPGA makes the image acquisition module highly flexible. Researchers can reconfigure the FPGA to implement specific image processing algorithms or functions based on specific application needs. This reconfigurability makes the FPGA-based image acquisition module suitable for multiple fields and application scenarios.

To sum up, the FPGA-based image acquisition module has the advantages of parallel computing capabilities, real-time performance and reconfigurability, making it an ideal choice for achieving high-quality, high-performance image acquisition and processing. Through in-depth research and development of FPGA technology, we can further promote the development of the field of digital image processing and provide more advanced solutions for various industries[4].

*2100257968@qq.com

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Significance: Humans obtain important information through images, so this module has a wide range of applications. In recent years, with the development of digital technology and the popularization of programmable chips, new developments have occurred in the design methods of image processing. At the same time, according to different applications in security, medical, military, industrial and other fields, the volumetric performance of the system has Requirements in terms of consumption, cost, miniaturization and operating speed are gradually becoming higher. Therefore, this research on the image acquisition module will be of great help to different fields.

2. BASIC COMPONENTS AND PRINCIPLES OF IMAGE ACQUISITION MODULE

This design uses simulation in Quartus II software based on FPGA, Verilog HDL language.

Quartus II is an integrated circuit design software suite developed by Intel Corporation for digital logic design, FPGA (Field Programmable Gate Array) design and verification[5]. It provides a comprehensive tool chain that supports the entire design flow from design input to layout, synthesis, timing optimization and generation of bitstream files. It supports Altera's IP core and includes LPM/MegaFunction macro function modules, allowing users to make full use of mature modules to simplify design complexity and speed up design. The following are some of the key features and capabilities of the Quartus II software:

Design input and verification: Quartus II provides a wealth of design input methods, including hardware description languages (such as Verilog HDL and VHDL), graphical design tools (such as Block Diagram/Schematic), system-level design (such as Qsys/Qsys Pro), etc.

Synthesis and layout: Quartus II software has advanced synthesis capabilities that synthesize hardware description language code into a logical netlist. It then performs place and route operations on the FPGA device, mapping the logical netlist to logic cells and programmable wires in the FPGA.

Timing analysis and optimization: Quartus II has powerful timing analysis and optimization functions that can help designers analyze and improve the timing performance of the design. It provides a variety of timing constraints and analysis tools to ensure that the design meets timing requirements, and provides timing optimization options to improve the timing performance of the design.

Special function and IP integration: Quartus II provides a wide range of special function modules and IP cores that can be easily integrated into the design, such as high-speed serial interfaces (such as PCIe, Ethernet), digital signal processing modules (such as FIR, FFT), embedded processor (such as Nios II), etc. These modules and IP cores can accelerate design development and reduce design complexity.

Configuration generation and download: Quartus II can generate an FPGA-specific configuration file (bitstream file) for loading the design into the target FPGA device. It also supports JTAG interface and other communication interfaces for downloading configuration files into FPGA devices for programming and debugging.

This module design mainly uses ADV7180 chip, camera OV5640, and SDRAM memory.

The hardware structure block diagram is shown in Figure 1:

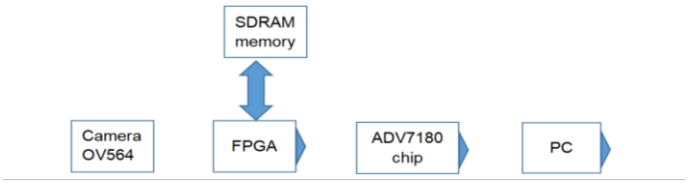

Figure 1. System hardware structure block diagram.

2.1 ADV7180 chip

In the design of image acquisition module based on FPGA, the function of ADV7180 chip is to convert analog video signals into digital video data. It is a video acquisition chip specially used to receive and process signals from analog video sources (such as cameras, DVDs, etc.) and convert them into digital video data for subsequent image processing, encoding, display, and other operations.

Specifically, the functions of the ADV7180 chip in the image acquisition module include:

Analog video signal reception: The ADV7180 chip can receive signals from analog video sources, such as composite video signals (Composite Video), S-video signals (S-Video), etc. It has a video input interface that can receive analog video signals by connecting a camera or other video source.

Analog to digital conversion: The ADV7180 chip contains an analog-to-digital converter (ADC) that converts analog video signals into digital data. It samples and quantizes the input analog video signal and converts it into digital video data for subsequent digital signal processing.

Video processing functions: The ADV7180 chip also has some video processing functions, such as noise reduction, color space conversion, sharpening, etc. These features help improve video quality and provide appropriate pre-processing based on application requirements.

Digital output interface: The ADV7180 chip provides digital video output interfaces, such as Pixel Data Bus, Sync Signals, etc. These digital video data can be received and processed through the input interface of the FPGA to complete subsequent image processing tasks, such as image enhancement, target detection, video encoding, etc.

In summary, the ADV7180 chip acts as a converter from analog video signals to digital video data in the image acquisition module. It is responsible for receiving, converting and processing analog video signals and providing digital video data for subsequent image processing and applications. By using the ADV7180 chip, analog video sources can be easily integrated into FPGA systems and perform flexible digital video processing.

The configuration logic of ADV7180 in the image module design is (Figure 2):

```
task configure_adv7180;
    begin
    // Send start condition to ADV7180 chip
    adv7180_sda <= 1'b1;
    adv7180_scl <= 1'b1;
    #1;
    adv7180_sda <= 1'b0;
    #1;
    adv7180_scl <= 1'b0;
    #1;
```

Figure 2. Configuration logic codes.

And the register parameter configuration of ADV7180 (Table 1):

Table 1. Table register parameter configuration.

Register parameter configuration										
Parameters	***Value***									
Register address	00h	04h	17h	31h	3dh	3e	3f	0e	55	0e
Set parameters	00	57	41	02	A2	6a	A0	80	81	00

2.2 Camera OV5640

In the design of image acquisition module based on FPGA and Verilog HDL language, the function of camera OV5640 is to realize the acquisition and transmission of image data. OV5640 is a commonly used high-performance CMOS image sensor that is widely used in embedded systems and digital image processing fields.

The main functions of the camera OV5640 in the image acquisition module include:

Image acquisition: Through its image sensor and optical system, the OV5640 can convert optical signals into digital image data. It captures high-resolution images and provides rich image settings and control options, such as exposure time, white balance, gain, etc.

Image transmission: OV5640 transmits the collected image data to the FPGA for processing and storage through the interface with the FPGA. It can communicate with FPGA through common interface protocols such as MIPI CSI-2, Parallel RGB and DVP.

Video stream processing: OV5640 can provide continuous video streaming data for real-time image processing and analysis. FPGA can process the received video stream data, such as filtering, image enhancement, target detection, etc.

System integration: OV5640 is a standard camera module that is easy to integrate with FPGA. It provides rich software drivers and development support and can be easily integrated with FPGA development environments, such as Quartus II. By using the OV5640, fast image acquisition and processing functions can be achieved.

In short, the camera OV5640 plays a key role in the design of the image acquisition module based on FPGA and Verilog HDL language. It is responsible for collecting image data and transmitting it to the FPGA, providing the basis for image processing and analysis for the system. The following is the configuration logic of OV5640 (Figure 3):

```
module ov5640_camera (
    input wire sys_clk,          // System clock input
    input wire reset,            // Reset signal input
    output wire [7:0] pixel      // Pixel data output
);
```

Figure 3. Configuration logic of OV5640.

2.3 Image sampling conversion

After the collected analog signal is A/D converted by ADV7180, 8-bit or 16-bit digital video and synchronization signals HS, VS, and FIELD will be output. Its internal registers are configured through the Altera chip.

The ADV7180 chip will correctly output the 8-bit video signal and synchronization signal HS, and VS will then convert the analog video signal into a digital video signal.

After the configuration of the ADV7180 is completed, the collected waveform will be observed using ModelSim. The waveform is as follows (Figure 4):

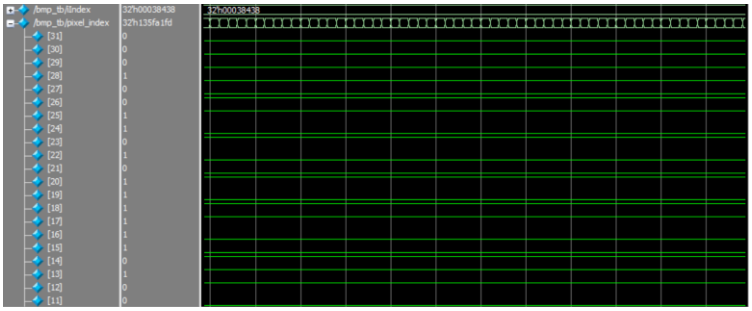

Figure 4. Image sampling conversion waveform.

After conversion by ADV7180, the standard YcrCb4:2:2 digital video is obtained. When used for display, we use 4:4 with 24 bits per pixel (8 bits for Y, Cb, and C each) data stream, so format conversion must be performed. During sampling, the chromaticity value (Cb and Cr) is only collected for every other pixel, so during conversion, the C and Cb values of the previous pixel with chromaticity information are directly assigned to the C of the next pixel. and Cb, so that 4:4:4 pixel data can be obtained. In addition, we also need to convert it into an RGB signal suitable for VGA monitors. Commonly used conversion formulas are as follow commonly used conversion formulas

$$Y=0.299R+0.587G+0.114B \quad (1)$$

$$Cb=0.564(B-Y) \quad (2)$$

$$Cr=0.713(R-Y) \quad (3)$$

$$R=Y+1.402Cr \quad (4)$$

$$G=Y-0.344Cb-0.714Cr \quad (5)$$

$$B=Y+1.772Cb \quad (6)$$

After the data is converted, the appropriate RGB format can be obtained. The controller is programmed according to the display timing to generate the display's horizontal synchronization information HS and field synchronization information VS, which are output to the display through the video interface.

The display waveform observed using ModelSim is shown in Figure 5.

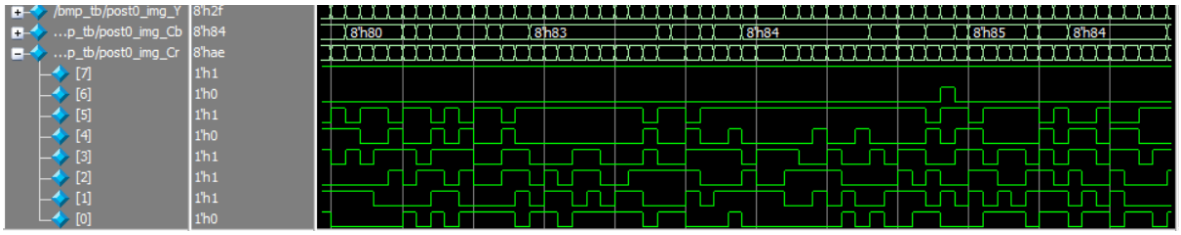

Figure 5. Result waveform.

As can be seen from Figure 5, after format conversion and RGB conversion output, a suitable video signal is obtained.

2.4 Image storage

Because the video data stream is large, real-time requirements are high. Therefore, high-speed and large-capacity memory is needed to cache image data. SDRAM has the advantages of large capacity and low price. Therefore, it is often used as a memory to store data in image processing. SDRAM memory modules typically contain some control logic to generate appropriate control, timing, and refresh signals[6]. This logic can be implemented in a hardware description language such as Verilog HDL or VHDL. The control of SDRAM is realized based on different combinations of control signals at the rising edge of the clock. The reading and writing process is shown in Figure 6.

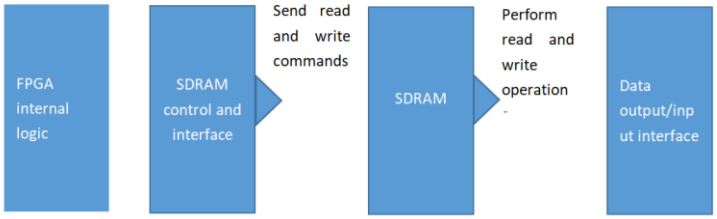

Figure 6. SDRAM read and write flow chart

The SDRAM read and write waveforms observed using modelsim are shown in Figure 7.

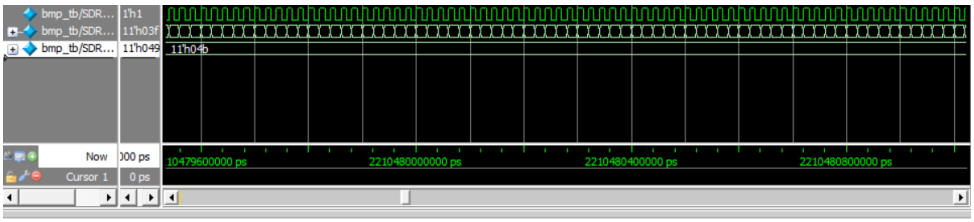

Figure 7. SDRAM read and write waveforms.

3. SUMMARY

3.1 Summary

This article describes the main process and results of the FPGA-based imaging module design. This module mainly utilizes the highly parallel processing capabilities and flexibility of FPGA to implement image processing.

First, we introduced the background and goals of the design. With the continuous development of digital imaging technology, the demand for real-time image processing is getting higher and higher. Traditional software implementation has performance bottlenecks when processing large-scale high-resolution images, and FPGA, as a hardware accelerator, can provide highly parallel computing capabilities to meet image processing requirements.

Next, we described in detail the FPGA architecture and key technologies adopted in the design. First, we selected an FPGA model suitable for image processing and evaluated its resources and performance. Then, we designed a data flow architecture adapted to the image processing algorithm, using the parallelism of FPGA to process multiple pixels simultaneously.

In terms of design implementation, we used ModelSim software for simulation and conducted comprehensive testing and verification. By comparing with traditional software implementations, we demonstrate significant improvements in performance of the FPGA-based imaging module. We conducted real-time demonstrations of various image processing algorithms and conducted quantitative and qualitative analysis of the processing results to verify the effectiveness and reliability of the design.

To sum up, the design of imaging module based on FPGA is a challenging research field with broad application prospects. Through reasonable architecture design and optimized algorithm implementation, we can use the powerful capabilities of FPGA to meet the needs of real-time image processing and contribute to the development of related fields[7,8].

4. CONCLUSION

FPGA-based imaging module design is an advanced module, and it will continue to play an important role in the future and continue to evolve with technological advancement and increasing demand. Through continuous innovation and optimization, we can expect to achieve higher performance and lower power consumption solutions in the field of real-time image processing, and make greater contributions to the application and development of related fields.

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