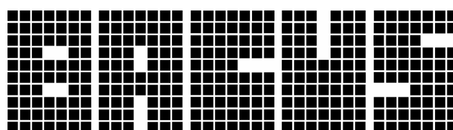
Photomask Technology 2007

Robert J. Naber
Hiroichi Kawahira
Editors

18–21 September 2007
Monterey, California, USA

Sponsored by



The international technical group of SPIE dedicated
to the advancement of photomask technology

Published by
SPIE

Volume 6730

Proceedings of SPIE, 0277-786X, v. 6730

SPIE is an international society advancing an interdisciplinary approach to the science and application of light.

The papers included in this volume were part of the technical conference cited on the cover and title page. Papers were selected and subject to review by the editors and conference program committee. Some conference presentations may not be available for publication. The papers published in these proceedings reflect the work and thoughts of the authors and are published herein as submitted. The publisher is not responsible for the validity of the information or for any outcomes resulting from reliance thereon.

Please use the following format to cite material from this book:
Author(s), "Title of Paper," in *Photomask Technology 2007*, edited by Robert J. Naber, Hiroichi Kawahira, Proceedings of SPIE Vol. 6730 (SPIE, Bellingham, WA, 2007) Article CID Number.

ISSN 0277-786X
ISBN 9780819468871

Published by
SPIE
P.O. Box 10, Bellingham, Washington 98227-0010 USA
Telephone +1 360 676 3290 (Pacific Time) · Fax +1 360 647 1445
SPIE.org

Copyright © 2007, Society of Photo-Optical Instrumentation Engineers

Copying of material in this book for internal or personal use, or for the internal or personal use of specific clients, beyond the fair use provisions granted by the U.S. Copyright Law is authorized by SPIE subject to payment of copying fees. The Transactional Reporting Service base fee for this volume is $18.00 per article (or portion thereof), which should be paid directly to the Copyright Clearance Center (CCC), 222 Rosewood Drive, Danvers, MA 01923. Payment may also be made electronically through CCC Online at copyright.com. Other copying for republication, resale, advertising or promotion, or any form of systematic or multiple reproduction of any material in this book is prohibited except with permission in writing from the publisher. The CCC fee code is 0277-786X/07/$18.00.

Printed in the United States of America.

Publication of record for individual papers is online in the SPIE Digital Library.

SPIEDigitalLibrary.org

Paper Numbering: Proceedings of SPIE follow an e-First publication model, with papers published first online and then in print and on CD-ROM. Papers are published as they are submitted and meet publication criteria. A unique, consistent, permanent citation identifier (CID) number is assigned to each article at the time of the first publication. Utilization of CIDs allows articles to be fully citable as soon they are published online, and connects the same identifier to all online, print, and electronic versions of the publication. SPIE uses a six-digit CID article numbering system in which:

- The first four digits correspond to the SPIE volume number.
- The last two digits indicate publication order within the volume using a Base 36 numbering system employing both numerals and letters. These two-number sets start with 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B … 0Z, followed by 10-1Z, 20-2Z, etc.

The CID number appears on each page of the manuscript. The complete citation is used on the first page, and an abbreviated version on subsequent pages. Numbers in the index correspond to the last two digits of the six-digit CID number.

Contents

Part One

xxiii	*Conference Committee*
xxvii	*Introduction*
xxix	*Schedule of Special Section on Double Patterning Lithography*
xxxi	*Summary of Special Section on Double Patterning Lithography*
xxxv	*PMJ Best Paper: Alternating phase-shift mask and binary mask for 45-nm node and beyond: the impact on the mask error control, Y. Kojima,M. Shirasaki, K. Chiba, T. Tanaka, Toppan Printing Co., Ltd. (Japan); Y. Inazuki, H. Yoshikawa, S. Okazaki, Shin-Etsu Chemical Co., Ltd. (Japan); K. Iwase, K. Ishikawa, K. Ozawa, Sony Corp.(Japan)*

SESSION 1 INVITED SESSION

6730 03 **Mask Industry Assessment: 2007** [6730-02]
G. Shelden, Shelden Consulting (USA); P. Marmillion, SEMATECH (USA) and IBM Corp. (USA); G. Hughes, SEMATECH (USA)

6730 04 **Compensating for image placement errors induced during the fabrication and chucking of EUVL masks (EMLC 2007 Best Paper)** [6730-03]
R. L. Engelstad, J. Sohn, A. R. Mikkelson, M. Nataraju, K. T. Turner, Univ. of Wisconsin, Madison (USA)

6730 06 **PMJ 2007 panel discussion overview: double exposure and double patterning for 32-nm half-pitch design node** [6730-05]
Y. Nagaoka, KLA-Tencor Japan Ltd. (Japan); H. Watanabe, Toshiba Corp. (Japan)

SESSION 2 ETCH

6730 07 **Characterizing photomask etch processes by phase component analysis (PCA)** [6730-06]
R. Wistrom, IBM System and Technology Group (USA); T. Komizo, Toppan Electronics Inc. (USA); M. Hibbs, G. Reid, IBM System and Technology Group (USA)

6730 08 **The advanced mask CD MTT control using dry etch process for sub 65 nm tech** [6730-07]
S. J. Jo, H. Y. Jung, D. W. Lee, J. C. Shin, J. Y. Jun, T. J. Ha, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 0A **CD bias control with in-situ plasma treatment in EPSM photomask etch** [6730-09]
K. Yung, C. J. Choi, K.-H. Baik, Intel Corp. (USA)

SESSION 3 SUBSTRATE

6730 0B **Effects of exposure environment on pellicle degradation in ArF lithography** [6730-10]
H. Choi, Y. Ahn, J. Yoon, Y. Lee, Y. Cho, J. Kim, Samsung Electronics Co., Ltd. (South Korea)

6730 0C **Development and characterization of a new low stress molybdenum silicide film for 45 nm attenuated phase-shift mask manufacturing** [6730-11]
T. Faure, E. E. Gallagher, L. Kindt, S. Nash, K. Racette, R. Wistrom, IBM Systems and Technology Group (USA); T. Komizo, Y. Kikuchi, S. Nemoto, Y. Sasaki, Toppan Electronics, Inc. (USA); A. Kominato, T. Suzuki, HOYA Corp. (Japan)

6730 0D **Evaluation of the effect of mask-blank flatness on CDU and DOF in high-NA systems** [6730-12]
C. Lee, Corning Tropel Corp. (USA); C. W. Chang, T. Chin, R. Lu, S. Fan, D. Chen, Nanya Technology Corp. (Taiwan); G. Chan, T. Huang, Toppan Chunghwa Electronics Co., Ltd. (Taiwan)

SESSION 4 IMPRINT

6730 0E **The development of full field high resolution imprint templates** [6730-13]
S. Yoshitake, H. Sunaoshi, K. Yasui, NuFlare Technology, Inc. (Japan); H. Kobayashi, T. Sato, O. Nagarekawa, HOYA Corp. (Japan); E. Thompson, G. Schmid, D. J. Resnick, Molecular Imprints, Inc. (USA)

6730 0F **Defect reduction progress in step and flash imprint lithography** [6730-14]
K. Selenidis, J. Maltabes, I. McMackin, J. Perez, W. Martin, D. J. Resnick, Molecular Imprints, Inc. (USA); S. V. Sreenivasan, Molecular Imprints, Inc. (USA) and Univ. of Texas at Austin (USA)

6730 0G **Fabrication of nano-imprint templates for dual-Damascene applications using a high resolution variable shape E-beam writer** [6730-15]
M. Pritschow, J. Butschke, M. Irmscher, H. Sailer, IMS Chips (Germany); D. Resnick, E. Thompson, Molecular Imprints, Inc. (USA)

SESSION 5 RESIST

6730 0H **The study of CD error in mid-local pattern area caused by develop loading effect** [6730-16]
M.-K. Kang, J.-H. Lee, S.-Y. Kim, B.-G. Kim, S.-G. Woo, H.-K. Cho, Samsung Electronics, Co. Ltd. (South Korea)

6730 0I **Performance improvement of ALTA4700 for 130nm and below mask productivity** [6730-17]
J. W. Hsu, D. Lee, C. R. Tseng, E. Hong, C. H. Wu, Taiwan Mask Corp. (Taiwan)

6730 0J **The behavior of substrate dependency as surface treatment in the positive chemically amplified resist** [6730-18]
S.-J. Yang, S&S Tech Corp. (South Korea); H.-S. Cha, Hanyang Univ. (South Korea); J.-H. Kang, C.-K. Yang, S&S Tech Corp. (South Korea); J.-H. Ahn, Hanyang Univ. (South Korea); K.-S. Nam, S&S Tech Corp. (South Korea)

6730 0K **Design for CD correction strategy using a resist shrink method via UV irradiation for defect-free photomask** [6730-19]
J. H. Ryu, D. W. Lee, H. Y. Jung, S. P. Kim, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 0L **The impact of mask photoresist develop on critical dimension parameters** [6730-20]
A. C. Smith, D. B. Sullivan, IBM System and Technology Group (USA); K. Sugawara, Y. Okawa, Toppan Electronics Inc. (USA)

SESSION 6 DFM 1: MASKS AND MANUFACTURABILITY

6730 0M **New method of contour-based mask-shape compiler** [6730-21]
R. Matsuoka, A. Sugiyama, A. Onizawa, H. Sato, Hitachi High-Technologies Corp. (Japan); Y. Toyoda, Hitachi, Ltd. (Japan)

6730 0N **Development of mask-DFM system MiLE load estimation of mask manufacturing** [6730-23]
Y. Nagamura, K. Hosono, Renesas Technology Corp. (Japan); S. Narukawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); M. Kato, H. Kawase, Keirex Technology Inc. (Japan)

6730 0O **DFM for maskmaking: design-aware flexible mask-defect analysis** [6730-24]
F. A. J. M. Driessen, J. Westra, M. Scheffer, K. Kawakami, Takumi Technology Corp. (Japan); E. Tsujimoto, M. Yamaji, T. Kawashima, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

6730 0P **Use of layout automation and design-based metrology for defect test mask design and verification** [6730-25]
C. Spence, C. Tabery, AMD (USA); A. Poock, AMD Fab 36 LLC & Co. KG (Germany); A. C. Duerr, T. Witte, J. Fiebig, J. Heumann, AMTC GmbH & Co. KG (Germany)

SESSION 7 DFM 2: MANUFACTURING MODELS AND PHYSICAL DESIGN

6730 0Q **Intel's AMT enables rapid processing and info-turn for Intel's DFM test chip vehicle** [6730-26]
H. Hajj, Intel Corp. (USA)

6730 0R **From rule to model-based design: A need for DfP criteria?** [6730-27]
A. Balasinski, Cypress Semiconductor (USA); N. Kachwala, D. Abercrombie, Mentor Graphics Inc. (USA)

6730 0S **Accurate lithography analysis for yield prediction** [6730-28]
G. Yeric, B. Hatamian, R. Kapoor, Synopsys, Inc. (USA)

6730 0T **Production-worthy full chip image-based verification** [6730-29]
Z. Yu, Y. Zhang, Y. Xiao, W. Li, Brion Technologies (USA)

6730 0U **Layout verification in the era of process uncertainty: requirements for speed, accuracy, and process portability** [6730-30]
J. A. Torres, Mentor Graphics Corp. (USA); I. Graur, IBM Systems and Technology Group (USA); M. C. Simmons, S. Kanodia, Mentor Graphics Corp. (USA)

SESSION 8 DFM 3: MODAL AWARE DESIGN AND OPTIMIZATION

6730 0V **A lithography aware design optimization using foundry-certified models and hotspot detection** [6730-36]
L. Karklin, A. Arkhipov, D. Blakely, M. Dingenen, A. Mehrotra, B. Watson, C. Zelnik, Sagantec (USA); M. Cote, P. Hurat, Clear Shape Technologies (USA)

6730 0W **Litho-aware extraction for the 32nm double patterning node** [6730-32]
J. Huckabay, Q. Chen, C. Thayer, R. Naber, Cadence Design Systems, Inc. (USA)

6730 0X **Silicon-verified automatic DFM layout optimization: a calibration-lite model-based application to standard cells** [6730-33]
K.-K. Lin, B. P. Wong, Chartered Semiconductor Manufacturing, Inc. (USA);
F. A. J. M. Driessen, E. Morita, S. Klaver, Takumi Technology Corp. (USA)

6730 0Y **Non-uniform yield optimization for integrated circuit layout** [6730-34]
F. G. Pikus, J. A. Torres, Mentor Graphics Corp. (USA)

6730 10 **Lateral interactions between standard cells using pattern matching** [6730-136]
L. T.-N. Wang, A. R. Neureuther, Univ. of California, Berkeley (USA)

6730 11 **Selecting and using a lithography compliance DFM tool for 65-nm foundry production** [6730-31]
B. Hatamian, R. Kapoor, Synopsys (USA)

SESSION 9 EUV AND OGL

6730 12 **Investigation of mask defectivity in full field EUV lithography** [6730-37]
R. Jonckheere, F. Iwamoto, G. F. Lorusso, A. M. Goethals, K. Ronse, IMEC vzw (Belgium);
H. Koop, T. Schmoeller, Synopsys GmbH (Germany)

6730 13 **Detectability and printability of EUVL mask blank defects for the 32-nm HP node** [6730-38]
W. Cho, SEMATECH MBDC (USA); H.-S. Han, SEMATECH (USA); K. A. Goldberg, Lawrence Berkeley National Lab. (USA); P. A. Kearney, C.-U. Jeon, SEMATECH MBDC (USA)

6730 14 **Measuring and characterizing the nonflatness of EUVL reticles and electrostatic chucks** [6730-39]
R. L. Engelstad, K. T. Turner, M. Nataraju, J. Sohn, A. R. Mikkelson, V. S. Battula, P. Vukkadala, J. R. Zeuske, Univ. of Wisconsin, Madison (USA); C. K. Van Peski, SEMATECH (USA)

6730 15 **Recent performance of EUV mask blanks with low-thermal expansion glass substrates** [6730-40]
T. Shoki, T. Yamada, S. Shimojima, Y. Shiota, M. Tsukahara, K. Koike, H. Shishido, O. Nozawa, T. Sakamoto, M. Hosoya, HOYA Corp. (Japan)

6730 16 **Investigation of resist effects on EUV mask defect printability** [6730-41]
Z. Zhang, T. Liang, Intel Corp. (USA)

6730 17 **Impact of mask absorber properties on printability in EUV lithography** [6730-42]
T. Kamo, H. Aoyama, T. Tanaka, O. Suga, MIRAI-Semiconductor Leading Edge Technologies, Inc. (Japan)

SESSION 10 CLEANING I

6730 18 **Capability of eco-friendly cleaning strategy corresponding to advanced technology** [6730-165]
S. Jeong, D. Lee, J. Ryu, J. Ryu, S. Kim, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 19 **Compositional analysis of progressive defects on a photomask** [6730-44]
K. Saga, H. Kawahira, Sony Corp. (Japan)

6730 1A **A practical solution to the critical problem of 193 nm reticle haze** [6730-45]
O. Kishkovich, D. Halbmaier, X. Gabarre, Entegris, Inc. (USA); B. Grenon, Grenon Consulting Inc. (USA); J. Lo, Entegris, Inc. (USA); A. Lam, T. Chen, Inotera Memories Inc. (USA)

6730 1B **Rapid and precise monitor of reticle haze** [6730-46]
T. Zavecz, TEA Systems Corp. (USA); B. Kasprowicz, Photronics, Inc. (USA)

SESSION 11 CLEANING II

6730 1D **Investigation of airborne molecular contamination adsorption rate as storage materials in mask** [6730-48]
C.-K. Yang, S&S Tech Corp. (South Korea); H.-S. Cha, Hanyang Univ. (South Korea); S.-J. Yang, J.-H. Kang, S&S Tech Corp. (South Korea); J.-H. Ahn, Hanyang Univ. (South Korea); K.-S. Nam, S&S Tech Corp. (South Korea)

6730 1E **Study of time dependent 193 nm reticle haze** [6730-49]
J. Gordon, L. Frisa, C. Chovino, D. Chan, J. Keagy, C. Weins, Toppan Photomasks, Inc. (USA)

6730 1F **Full sulfate-free process: joint achievement of minimal residual ions and yield improvement** [6730-50]
F. Perissinotti, L. Sartelli, D. Cassago, H. Miyashita, DNP Photomask Europe (Italy)

SESSION 12 EXTREME NA

6730 1G **Using the AIMS 45-193i for hyper-NA imaging applications** [6730-51]
P. De Bisschop, V. Philipsen, IMEC (Belgium); R. Birkner, U. Buttgereit, R. Richter, T. Scherübl, Carl Zeiss SMS GmbH (Germany)

6730 1H **Mask characterization for double patterning lithography** [6730-52]
K. Bubke, E. Cotte, J. H. Peters, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany); R. de Kruif, ASML Netherlands B.V. (Netherlands); M. Dusa, ASML US, Inc. (USA); J. Fochler, B. Connolly, Toppan Photomasks, Inc. (Germany)

6730 1I **DPL performance analysis strategy with conventional workflow** [6730-53]
N. Toyama, Y. Inazuki, T. Sutou, T. Nagai, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); J. Miyazaki, ASML Japan (Japan); A. Chen, ASML Taiwan (Taiwan); N. Samarakone, ASML USA (USA)

6730 1J **Estimating DPL photomask fabrication load compared with single exposure** [6730-54]
N. Toyama, Y. Inazuki, T. Sutou, T. Nagai, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); J. A. Huckabay, Cadence Design Systems, Inc. (USA); Y. Abe, Cadence Design Systems, Inc. (Japan)

6730 1L **Pattern split rules! A feasibility study of rule based pitch decomposition for double patterning** [6730-152]
A. van Oosten, P. Nikolsky, ASML Netherlands B.V. (Netherlands); J. Huckabay, Cadence Design Systems (USA); R. Goossens, ASML MaskTools Inc. (USA); R. Naber, Cadence Design Systems (USA)

6730 1M **The MEEF NILS divergence for low k1 lithography** [6730-56]
R. Schenker, W. Cheng, G. Allen, Intel Corp. (USA)

6730 1N **Impact of alternative mask stacks on the imaging performance at NA 1.20 and above** [6730-57]
V. Philipsen, K. Mesuda, P. De Bisschop, IMEC (Belgium); A. Erdmann, G. Citarella, P. Evanschitzky, Fraunhofer IISB (Germany); R. Birkner, R. Richter, T. Scherübl, Carl Zeiss SMT (Germany)

6730 1O **Requirements of photomask registration for the 45nm node and beyond: Is it possible?** [6730-58]
J. Choi, H. B. Kim, S. H. Lee, D. H. Lee, H. Y. Jeong, J. W. Lee, B. G. Kim, S.-G. Woo, H. K. Cho, Samsung Electronics Co., Ltd. (South Korea)

SESSION 13 SIMULATION

6730 1P **Simulation of larger mask areas using the waveguide method with fast decomposition technique** [6730-59]
P. Evanschitzky, F. Shao, A. Erdmann, D. Reibold, Fraunhofer Institute of Integrated Systems and Device Technology (Germany)

6730 1Q **Polarization aberration modeling via Jones matrix in the context of OPC** [6730-60]
Q. Zhang, H. Song, K. Lucas, Synopsys, Inc. (USA)

6730 1R **Validation of a fast and accurate 3D mask model for SRAF printability analysis at 32nm node** [6730-61]
P. Liu, C. Zuniga, Brion Technologies, Inc. (USA); Z. Ma, Brion Technologies Co., Ltd. (China); H. Feng, Brion Technologies, Inc. (USA)

6730 1S **Fast three-dimensional simulation of buried EUV mask defect interaction with absorber features** [6730-62]
C. H. Clifford, A. R. Neureuther, Univ. of California, Berkeley (USA)

6730 1T **Polarization-induced astigmatism caused by topographic masks** [6730-63]
J. Ruoff, J. T. Neumann, Carl Zeiss SMT AG (Germany); E. Schmitt-Weaver, ASML US, Inc. (USA); E. van Setten, N. le Masson, ASML Netherlands (Netherlands); C. Progler, Photronics, Inc. (USA); B. Geh, Carl Zeiss SMT AG (Germany) and ASML US, Inc. (USA)

6730 1U **Characterization and monitoring of photomask edge effects** [6730-64]
M. A. Miller, A. R. Neureuther, D. P. Ceperley, J. Rubinstein, K. Kikuchi, Univ. of California, Berkeley (USA)

6730 1W **EMF simulations of isolated and periodic 3D photomask patterns** [6730-163]
S. Burger, L. Zschiedrich, F. Schmidt, Zuse Institute Berlin (Germany) and JCMwave GmbH (Germany); R. Köhle, Qimonda AG (Germany); B. Küchler, C. Nölscher, Qimonda Dresden GmbH & Co. OHG (Germany)

6730 1X **Fast and accurate laser bandwidth modeling of optical proximity effects** [6730-66]
I. Lalovic, Cymer, Inc. (USA); O. Kritsun, Advanced Micro Devices (USA); J. Bendik, Dynamic Intelligence Inc. (USA); M. Smith, C. Sallee, KLA-Tencor Corp. (USA); N. Farrar, Cymer, Inc. (USA)

Part Two

SESSION 14 REPAIR I

6730 1Y **Advanced mask particle cleaning solutions** [6730-67]
T. Robinson, A. Dinsdale, R. Bozak, B. Arruza, RAVE, LLC (USA)

6730 1Z **Integrated photomask defect printability check, mask repair, and repair validation procedure for phase-shifting masks for the 45-nm node and beyond** [6730-68]
C. Ehrlich, U. Buttgereit, K. Boehm, T. Scheruebl, Carl Zeiss SMS GmbH (Germany); K. Edinger, T. Bret, Nawotec GmbH (Germany)

SESSION 15 REPAIR II

6730 20 **A semi-automated AFM photomask repair process for manufacturing application using SPR6300** [6730-69]
M. Dellagiovanna, H. Yoshioka, H. Miyashita, DNP Photomask Europe SpA. (Italy); S. Murai, Dai Nippon Printing Co., Ltd. (Japan); T. Nakaue, O. Takaoka, A. Uemoto, S. Kikuchi, R. Hagiwara, SII NanoTechnology Inc. (Japan); S. Benard, Bs Technology eurl (France)

6730 21 **Repairing 45 nm node defects through nano-machining** [6730-70]
R. White, A. Dinsdale, T. Robinson, D. Brinkley, J. Csuy, D. Lee, RAVE LLC (USA)

6730 22 **The cleaning effects of mask aerial image after FIB repair in sub-80nm node** [6730-71]
H. Lee, G. Jeong, S. Jeong, S. Kim, O. Han, Hynix Semiconductor Inc. (South Korea)

SESSION 16 INSPECTION

6730 23 **Wafer inspection as alternative approach to mask defect qualification** [6730-72]
C. Holfeld, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany); F. Katzwinkel, U. Seifert, Qimonda Dresden GmbH & Co. OHG (Germany); A. Mothes, J. H. Peters, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany)

6730 24 **A pragmatic approach to high sensitivity defect inspection in the presence of mask process variability** [6730-73]
S. H. Han, J. H. Park, D. H. Chung, S.-G. Woo, H. K. Cho, Samsung Electronics, Co. Ltd. (South Korea); D. Kim, C. Chen, K.-H. Park, G. Inderhees, KLA-Tencor Corp. (USA)

6730 25 **Sensitivity comparison of fast integrated die-to-die T+R pattern inspection, standard database inspection, and STAR*light2* contamination mode for application in mask production** [6730-74]
H. Schmalfuss, KLA-Tencor Corp. (USA); T. Schulmeyer, J. Heumann, Advanced Mask Technology Ctr. Inc. (Germany); M. Lang, J.-P. Sier, KLA-Tencor Corp. (USA)

6730 26 **Enhancing productivity and sensitivity in mask production via a fast integrated die-to-database T+R inspection** [6730-129]
E. H. Lu, KLA-Tencor Corp. (USA); D. Wu, E. Chen, KLA-Tencor Corp. (Taiwan); R. Badoni, KLA-Tencor Corp. (USA)

6730 27 **Progressive growth and hard defect disposition integrated system for 65nm and 45nm ArF immersion lithography** [6730-76]
G. S. Chua, S. K. Tan, B. I. Choi, O. Y. Lee, J. S. Kim, Chartered Semiconductor Manufacturing Ltd. (Singapore)

6730 28 **Characterizing contamination inspection capabilities using programmed defect test reticles** [6730-77]
A. Nhiev, J. Riddick, J. Straub, Toppan Photomasks (USA); T. Hutchinson, B. Reese, A. Dayal, KLA-Tencor Corp. (USA)

6730 29 **Mask inspection method for 45nm node device** [6730-78]
S. Oh, Y. Choi, D. Hwang, G. Jeong, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 2A **Inspection results for 32nm logic and sub-50nm half-pitch memory reticles using the TeraScanHR** [6730-79]
J.-P. Sier, W. Broadbent, F. Mirzaagha, P. Yu, KLA-Tencor Corp. (USA)

6730 2B **Automatic optimization of MEEF-driven defect disposition for contamination inspection challenges** [6730-80]
T. Huang, A. Dayal, K. Bhattacharyya, J. Huang, KLA-Tencor Corp. (USA); W. Chou, Y.-F. Cheng, S.-M. Yen, J. Cheng, P. Peng, United Microelectronics Corp. (Taiwan)

SESSION 16 ADVANCED RET

6730 2C **Paving the way to a full chip gate level double patterning application** [6730-81]
H. Haffner, Infineon Technologies NA Corp. (USA); J. Meiring, Z. Baum, S. Halle, IBM Semiconductor Research and Development Ctr. (USA)

6730 2E **Automatic assist feature placement optimization based on process-variability reduction** [6730-83]
S. Jayaram, Mentor Graphics Corp. (USA); A. Yehia, M. Bahnas, H. A. Maaty Omar, Mentor Graphics Corp. (Egypt); Z. Bozkus, J. L. Sturtevant, Mentor Graphics Corp. (USA)

6730 2F **Full-chip-based subresolution assist features correction for mask manufacturing** [6730-84]
J.-M. Bang, Samsung Electronics Co., Ltd. (South Korea); I. Masumoto, Nippon Control System Co. (Japan); M.-K. Ji, S.-H. Jang, Samsung Electronics Co., Ltd. (South Korea); I. Aburatani, Nippon Control System Co. (Japan); J.-H. Choi, S.-G. Woo, H.-K. Cho, Samsung Electronics Co., Ltd. (South Korea)

6730 2G **Etch proximity correction by integrated model-based retargeting and OPC flow** [6730-85]
S. Shang, Y. Granik, Mentor Graphics Corp. (USA); M. Niehoff, Mentor Graphics Corp. (Germany)

6730 2H **Resolution enhancement by aerial image approximation with 2D-TCC** [6730-86]
K. Yamazoe, Y. Sekine, M. Kawashima, M. Hakko, T. Ono, T. Honda, Canon Inc. (Japan)

SESSION 17 RET I

6730 2I **Exploring the sources of MEEF in contact SRAMs** [6730-87]
E. Gallagher, I. Stobert, IBM Corp. (USA); M. Higuchi, Toppan Electronics Inc. (USA); D. Samuels, IBM Corp. (USA)

6730 2J **The improvement of OPC accuracy and stability by the model parameters' analysis and optimization** [6730-88]
N.-Y. Chung, W.-H. Choi, S.-H. Lee, S.-I. Kim, S.-Y. Lee, Samsung Electronics Co., Ltd. (South Korea)

6730 2K **Simultaneous model-based main feature and SRAF optimization for 2D SRAF implementation to 32 nm critical layers** [6730-186]
A. Yehia, Mentor Graphics Corp. (Egypt); A. Tritchkov, Mentor Graphics Corp. (USA)

6730 2M **A generic technique for reducing OPC iteration: fast forward OPC** [6730-187]
L. Hong, J. Sturtevant, Mentor Graphics Corp. (USA)

6730 2N **Fast synthesis of topographic mask effects based on rigorous solutions** [6730-91]
Q. Yan, Z. Deng, J. Shiely, Synopsys, Inc. (USA)

SESSION 18 RET II

6730 2O **Improving hyper-NA OPC using targeted measurements for model parameter extraction** [6730-92]
B. S. Ward, IMEC (Belgium)

6730 2P **Selective process aware OPC for memory device** [6730-93]
W. Shim, S. Suh, Samsung Electronics Co., Ltd. (South Korea); F. Amoroso, R. Lugg, S. Lee, Synopsys, Inc. (USA); S. Lee, S.-H. Oh, J. Lee, T.-H. Ahn, C.-J. Kang, Samsung Electronics Co., Ltd. (South Korea)

6730 2Q **Validating optical proximity correction with models, masks and wafers** [6730-94]
S. Marokkey, Infineon Technologies AG (USA); E. W. Conrad, E. E. Gallagher, IBM System and Technology Group (USA); H. Ikeda, Toppan Electronics, Inc. (USA); J. A. Bruce, M. Lawliss, IBM System and Technology Group (USA)

6730 2R **The study of phase-angle and transmission specifications of 6% att-EAPSM for 90nm, 65nm, and 45nm node wafer manufacturing patterning process** [6730-95]
G. Chen, C. Garza, Freescale Semiconductor, Inc. (USA)

6730 2S **Better on wafer performance and mask manufacturability of contacts with no or non-traditional serifs** [6730-96]
D. Samuels, I. Stobert, IBM Semiconductor Research and Development Ctr. (USA)

6730 2T **Optimization of OPC runtime using efficient optical simulation** [6730-97]
M. Al-Imam, W. A. Tawfic, Mentor Graphics Corp. (Egypt)

6730 2U **Full-chip process window aware OPC capability assessment** [6730-98]
R. Lugg, M. StJohn, Y. Zhang, A. Yang, P. Van Adrichem, Synopsys, Inc. (USA)

SESSION 19 MASK BUSINESS/MANAGEMENT

6730 2V **E-beam direct write is free** [6730-100]
L. A. Glasser, Consultant (USA)

6730 2W **Driving photomask supplier quality through automation** [6730-101]
D. Russell, A. Espenscheid, Freescale Semiconductor, Inc. (USA)

6730 2X **Multi-layer reticle (MLR) strategy application to double-patterning/double-exposure for better overlay error control and mask cost reduction** [6730-102]
Y. Yamamoto, Cadence Design Systems, Japan (Japan); R. Rigby, J. Sweis, Cadence Design Systems, Inc. (USA)

SESSION 20 PATTERNING

6730 2Y **Polygon-based compensation of proximity and density effects in photomask processes** [6730-103]
K. Kageyama, K. Miyoko, Y. Okuda, Toppan Printing Co., Ltd. (Japan); G. Perçin, Invarium, Inc. (USA); A. Sezginer, J. Carrero, A. Zhu, A. Liu, Cadence Design Systems, Inc. (USA)

6730 2Z **Improvement of mask CD uniformity for below 45-nm node technology** [6730-104]
H. Lee, S. Bae, J. Park, D. Nam, B. Kim, S.-G. Woo, H. Cho, Samsung Electronics Co., Ltd. (South Korea)

6730 30 **Correction technique of EBM-6000 prepared for EUV mask writing** [6730-105]
S. Yoshitake, H. Sunaoshi, J. Yashima, S. Tamamushi, NuFlare Technology Inc. (Japan); M. Ogasawara, Toshiba Corp. (Japan)

6730 31 **Coping with double-patterning/exposure lithography by EB mask writer EBM-6000** [6730-106]
T. Kamikubo, R. Nishimura, K. Tsuruta, K. Hattori, J. Takamatsu, S. Yoshitake, H. Nozue, H. Sunaoshi, S. Tamamushi, NuFlare Technology, Inc. (Japan)

6730 32 **Performance comparison of techniques for intra-field CD control improvement** [6730-107]
R. Pforr, M. Hennig, J. Reichelt, Qimonda Dresden GmbH & Co. OHG (Germany); G. Ben Zvi, Pixer Technology Ltd. (Israel); M. Sczyrba, Advanced Mask Technology Ctr. (Germany)

6730 33 **Projection maskless patterning (PMLP) for the fabrication of leading-edge complex masks and nano-imprint templates** [6730-108]
E. Platzgummer, H. Loeschner, G. Gross, IMS Nanofabrication AG (Austria)

6730 34 **Improving the CD linearity and proximity performance of photomasks written on the Sigma7500-II DUV laser writer through embedded OPC** [6730-109]
A. Österberg, L. Ivansen, A. Beyerl, T. Newman, Micronic Laser Systems AB (Sweden); A. Bowhill, E. Sahouria, S. Schulze, Mentor Graphics Corp. (USA)

6730 35 **Contrast properties of spatial light modulators for microlithography** [6730-110]
J. Heber, D. Kunze, P. Dürr, D. Rudloff, M. Wagner, Fraunhofer Institut für Photonische Mikrosysteme (Germany); P. Björnängen, J. Luberek, U. Berzinsh, T. Sandström, T. Karlin, Micronic Laser Systems AB (Sweden)

SESSION 21 METROLOGY I

6730 36 **Accuracy of mask pattern contour extraction with fine-pixel SEM images** [6730-111]
S. Yamaguchi, E. Yamanaka, H. Mukai, T. Kotani, H. Mashita, M. Itoh, Toshiba Corp. (Japan)

6730 37 **2D measurement using CD SEM for arbitrarily shaped patterns** [6730-112]
H.-J. Lee, S.-Y. Bae, D.-H. Chung, S.-G. Woo, H. Cho, Samsung Electronics Co., Ltd. (South Korea); J. Matsumoto, T. Nakamura, Advantest Corp. (Japan); D. Shin, T. Kim, Vistec Semiconductor Systems Pte. Ltd. (South Korea)

SESSION 22 METROLOGY II

6730 39 **Images in photoresist for self-interferometric electrical image monitors** [6730-177]
J. Rubinstein, A. R. Neureuther, Univ. of California, Berkeley (USA)

6730 3A **Preliminary verifiability of the aerial image measurement tool over photolithography process** [6730-114]
H. Lee, G. Jeong, S. Kim, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 3B **Calibration of contact areas: the influence of corner rounding** [6730-115]
J. Richter, E.-M. Zerbe, T. Marschner, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany)

6730 3C **Measurements of corner rounding in 2D contact holes on phase-shift masks using broadband reflectance and transmittance spectra in conjunction with RCWA** [6730-116]
A. Gray, Univ. of California, Davis (USA); J. C. Lam, S. Chen, n&k Technology, Inc. (USA); J. Richter, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany)

6730 3D **Photomask applications of traceable atomic force microscope dimensional metrology at NIST** [6730-117]
R. Dixson, N. G. Orji, J. Potzick, J. Fu, R. A. Allen, M. Cresswell, National Institute of Standards and Technology (USA); S. Smith, A. J. Walton, A. Tsiamis, Univ. of Edinburgh (United Kingdom)

6730 3E **Laterally resolved off-axis phase measurements on 45-nm node production features using Phame** [6730-118]
U. Buttgereit, S. Perlitz, D. Seidel, Carl Zeiss SMS GmbH (Germany); K. M. Lee, M. Tavassoli, Intel Mask Operation (USA)

SESSION 23 MDP

6730 3F **LRC techniques for improved error detection throughout the process window** [6730-119]
V. Lee, S.-H. Tsai, United Microelectronics Corp. (Taiwan); J. Zhu, L. Wang, S.-M. Yang, D. White, Synopsys, Inc. (USA)

6730 3G **Teracomputing for mask data preparation** [6730-120]
J. Nogatch, H. Kirsch, K. Mostafa, G. Newell, J. Yeap, Synopsys, Inc. (USA)

6730 3I **Compressing MEBES data enabling multi-threaded decompression** [6730-155]
M. Pereira, A. Parchuri, SoftJin Technologies Pvt. Ltd. (India)

6730 3J **Mask manufacturability improvement by MRC** [6730-122]
A. Balasinski, D. Coburn, Cypress Semiconductor (USA); P. Buck, Toppan Photomask, Inc. (USA)

6730 3K **Reduction of layout complexity for shorter mask write-time** [6730-123]
S. Hannon, T. Lewis, S. Goad, Advanced Micro Devices, Inc. (USA); K. Jantzen, J. Wang, H. T. Vu, E. Sahouria, S. Schulze, Mentor Graphics Corp. (USA)

Part Three

POSTER SESSION: INSPECTION

6730 3L **Optimizing defect inspection strategy through the use of design-aware database control layers** [6730-75]
D. Stoler, W. Ruch, W. Ma, S. Chakravarty, S. Liu, KLA-Tencor (USA); R. Morgan, J. Valadez, B. Moore, J. Burns, Synopsys, Inc. (USA)

6730 3M **New method of identification of false or nuisance defects using defect imaging system DIS-05** [6730-124]
H. Zhang, K. Takahashi, H. Bando, Y. Kitayama, A. Sugano, K. Kobayashi, Holon Co., Ltd. (Japan)

6730 3O **Improving inspectability with KLA-Tencor TeraScan thin line de-sense** [6730-126]
C. Chen, D. Kim, K. H. Park, N. Kim, KLA-Tencor Corp. (USA); S. H. Han, J. H. Park, D. H. Chung, Samsung Electronics Co., Ltd. (South Korea)

6730 3P **Implementation of an efficient defect classification method in photomask mass production** [6730-127]
C. Liu, C. Wang, S. Zhang, E. Guo, Semiconductor Manufacturing International Corp. (China); S. Liu, E. H. Lu, D. Fan, D. Wang, W. Ma, KLA-Tencor Corp. (USA)

6730 3Q **To improve reticle re-qualification process and reduce reticle re-cleaning frequency using efficient defect classification and defect tracking** [6730-128]
E. H. Lu, KLA-Tencor Corp. (USA); J. Wang, KLA-Tencor Corp. (Taiwan); R. Badoni, KLA-Tencor Corp. (USA); E. Chen, KLA-Tencor Corp. (Taiwan); W. Ma, KLA-Tencor Corp. (USA)

6730 3R **Automating defect disposition in fabs and maskshops** [6730-130]
P. Fiekowsky, Automated Visual Inspection (USA); S. Narukawa, T. Kawashima, Dai Nippon Printing Co., Ltd. (Japan)

POSTER SESSION: DESIGN FOR MANUFACTURABILITY (DFM)

6730 3S **Automatic OPC repair flow: optimized implementation of the repair recipe** [6730-132]
M. Bahnas, M. Al-Imam, Mentor Graphics Egypt (Egypt); J. Word, Mentor Graphics Corp. (USA)

6730 3T **Database and data analysis strategy for multi-designer testchips** [6730-133]
W. J. Poppe, P. Au, D. Jayasuriya, A. Neureuther, Univ. of California at Berkeley (USA)

6730 3V **Determining OPC target specifications electrically instead of geometrically** [6730-135]
Q. Zhang, P. van Adrichem, Synopsys, Inc. (USA)

6730 3W **Application of modified jog-fill DRC rule on LFD OPC flow** [6730-137]
Y.-M. Kim, S.-U. Lee, J.-H. Kang, J.-H. Kim, K.-H. Kim, DongbuHitek (South Korea)

POSTER SESSION: SUBSTRATE AND MATERIALS

6730 3Y **Pellicle dimensions for high NA photomasks** [6730-139]
F. Erber, T. Schulmeyer, C. Holfeld, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany)

6730 3Z **Evaluation of attenuated PSM photomask blanks with TF11 chrome and FEP-171 resist on a 248 nm DUV laser pattern generator** [6730-140]
K. Xing, C. Björnborg, H. Karlsson, A. Paulsson, A. Rosendahl, P. Beiming, J. Vedenpää, J. Walford, T. Newman, Micronic Laser Systems AB (Sweden)

POSTER SESSION: RESIST PROCESS AND ETCH

6730 40 **Bimetallic thermal resists potential for double-exposure immersion lithography and grayscale photomasks** [6730-141]
J. M. Dykes, C. Plesa, C. Choo, G. H. Chapman, Simon Fraser Univ. (Canada)

6730 42 **Acid diffusion length limitation for 45 nm node attenuated and chromeless phase shift mask** [6730-143]
Y.-M. Kang, S.-W. Park, H.-K. Oh, Hanyang Univ. (South Korea)

6730 43 **Critical dimension control for 32 nm random contact hole array with resist reflow process** [6730-144]
J.-M. Park, Y.-M. Kang, S.-W. Park, J.-Y. Hong, H.-K. Oh, Hanyang Univ. (South Korea)

6730 44 **Self-aligned resist patterning with 172nm and 193nm backside flood exposure on attenuated phase shift masks** [6730-145]
J. Chun, T. Ha, H. Jung, S. Jo, O. Han, Hynix Semiconductor Inc. (South Korea)

6730 45 **Practical use of hard mask process to fabricate fine photomasks for 45nm node and beyond** [6730-147]
Y. Kushida, H. Handa, H. Maruyama, Fujitsu Ltd. (Japan); Y. Abe, Y. Fujimura, T. Yokoyama, Dai Nippon Printing Co., Ltd. (Japan)

6730 46 **Overcoming loading challenges in a mask etcher for 45 nm and beyond** [6730-213]
M. Chandrachood, T. Y. B. Leung, K. Yu, M. Grimbergen, S. Panayil, I. Ibrahim, A. Sabharwal, A. Kumar, Applied Materials, Inc. (USA)

POSTER SESSION: PATTERNING

6730 47 **Resistless mask structuring using an ion multi-beam projection pattern generator** [6730-148]
J. Butschke, M. Irmscher, F. Letzkus, IMS Chips (Germany); H. Loeschner, IMS Nanofabrication AG (Austria); L. Nedelmann, IMS Chips (Germany); E. Platzgummer, IMS Nanofabrication AG (Austria)

6730 48 **Reconfigurable lithographic applications using polymer liquid crystal composite films** [6730-149]
A. E. Fox, A. K. Fontecchio, Drexel Univ. (USA)

6730 4A **Pattern density and process related CD corrections at 32nm node** [6730-151]
Z. Benes, IBM Systems and Technology Group (USA); J. Kotani, Toppan Electronics Inc. (USA)

POSTER SESSION: EXTREME NA/IMMERSION LITHOGRAPHY

6730 4B **Automatic residue removal for high-NA extreme illumination** [6730-153]
J. Moon, B.-S. Nam, J.-H. Jeong, D.-H. Kong, B.-H. Nam, D. G. Yim, Hynix Semiconductor Inc. (South Korea)

POSTER SESSION: MDP/MRC

6730 4C **Effective area partitioning for preparing parallel processing in mask data preparation** [6730-154]
Y. Satou, Y. Okamoto, M. Fujimoto, H. Tsuchida, A. Satou, TOOL Corp. (Japan)

6730 4D **Mask calibration dominated methodology for OPC matching** [6730-156]
L. Zhu, Shanghai Institute of Microsystem and Information Technology (China), Graduate School of Chinese Academy of Science (China), and Grace Semiconductor Manufacturing Corp. (China); M. Lu, D. King, Y. Gu, S. Yang, Grace Semiconductor Manufacturing Corp. (China); L. S. Melvin III, Synopsys, Inc. (USA)

6730 4E **Integration of OPC and mask data preparation for reduced data I/O and reduced cycle time** [6730-157]
R. Morgan, M. Chacko, D. Hung, J. Yeap, M. Boman, Synopsys, Inc. (USA)

6730 4F **Mask rule check using priority information of mask patterns** [6730-158]
K. Kato, Y. Taniguchi, K. Nishizawa, M. Endo, T. Inoue, R. Hagiwara, A. Yasaka, SII NanoTechnology Inc. (Japan)

6730 4G **Improving the efficiency of pattern extraction for character projection lithography using OPC optimization** [6730-159]
H. Nosato, National Institute of Advanced Industrial Science and Technology (Japan); T. Matsunawa, Univ. of Tsukuba (Japan); H. Sakanashi, M. Murakawa, National Institute of Advanced Industrial Science and Technology (Japan); T. Higuchi, National Institute of Advanced Industrial Science and Technology (Japan) and Univ. of Tsukuba (Japan)

6730 4H **A user-programmable link between data preparation and mask manufacturing equipment** [6730-160]
W. Zhang, G. Davis, E. Sahouria, S. Schulze, Mentor Graphics Corp. (USA); M. Saad, Mentor Graphics Corp. (Egypt); A. Seyfarth, Carl Zeiss SMS GmbH (Germany); E. Poortinga, Carl Zeiss SMT Inc. (USA)

POSTER SESSION: SIMULATION

6730 4I **32nm half pitch node OPC process model development for three dimensional mask effects using rigorous simulation** [6730-161]
L. S. Melvin III, Synopsys, Inc. (USA); T. Schmoeller, Synopsys, Inc. (Germany); J. Li, Synopsys, Inc. (USA)

6730 4J **OPC verification on cell level using fully rigorous mask topography simulation** [6730-162]
V. Domnenko, Synopsys, Inc. (Russia); T. Klimpel, G. Viehoever, H. Koop, Synopsys, Inc. (Germany); L. S. Melvin III, Synopsys, Inc. (USA); T. Schmoeller, Synopsys, Inc. (Germany)

POSTER SESSION: CLEANING

6730 4K **A study of haze generation as thin film materials** [6730-43]
J.-H. Kang, S&S Tech Corp. (South Korea); H.-S. Cha, Hanyang Univ. (South Korea); S.-J. Yang, C.-K. Yang, S&S Tech Corp. (South Korea); J.-H. Ahn, Hanyang Univ. (South Korea); K.-S. Nam, S&S Tech Corp. (South Korea); J.-M. Kim, M. Patil, I.-B. Hur, S.-S. Choi, Photronics-PKL (South Korea)

6730 4L **A method to determine the origin of remaining particles after mask blank cleaning** [6730-166]
V. Kapila, S. Eichenlaub, A. Rastegar, A. John, International SEMATECH (USA); P. Marmillion, SEMATECH (USA)

6730 4O **Haze generation effect by pellicle and packing box on photomask** [6730-170]
J.-M. Kim, M. Patil, W.-G. Jeong, I.-B. Hur, C. Shin, S.-M. Jung, M.-H. Choi, S.-S. Choi, PKL - Photronics (South Korea)

6730 4P **Laser shockwave cleaning of EUV reticles** [6730-171]
N. A. Lammers, Univ. of Technology Eindhoven (Netherlands); A. Bleeker, ASML (Netherlands)

6730 4Q **Mask protection from a haze during shipping and storage** [6730-172]
T. Umeda, Adhand, Inc. (Japan); H. Kawashima, Hakuto Co., Ltd. (Japan); T. Miho, Miraial Co., Ltd. (Japan); K. Moriya, Nippon Puretec Co., Ltd. (Japan)

POSTER SESSION: METROLOGY

6730 4R **CD-signature evaluation using scatterometry** [6730-173]
J. Richter, P. Laube, Advanced Mask Technology Ctr. GmbH & Co. KG (Germany); J. Lam, n&k Technology, Inc. (USA)

6730 4S **Parameter sensitive patterns for scatterometry monitoring** [6730-174]
J. Xue, Y. Ben, C. Wang, M. Miller, C. J. Spanos, A. R. Neureuther, Univ. of California, Berkeley (USA)

6730 4T **Long-term critical dimension measurement performance for a new mask CD-SEM, S-9380M** [6730-175]
Z. Wang, K. K. Seet, R. Fukaya, Y. Kadowaki, N. Arai, M. Ezumi, H. Satoh, Hitachi High-Technologies Corp. (Japan)

6730 4V **The study for close correlation of mask and wafer to optimize wafer field CD uniformity** [6730-179]
M. Kim, J. Kang, S. Kang, G. Jeong, Y. Choi, O. Han, Hynix Semiconductor (South Korea)

6730 4W **Development of a captured image simulator for the differential interference contrast microscopes aiming to design 199 nm mask inspection tools** [6730-180]
M. Shiratsuchi, Y. Honguh, Toshiba Corp. (Japan); R. Hirano, R. Ogawa, M. Hirono, Advanced Mask Inspection Technology (Japan); T. Nomura, NuFlare Technology, Inc. (Japan)

6730 4X **Mask CD control (CDC) with ultrafast laser for improving mask CDU using AIMS as the CD metrology data source** [6730-214]
G. Ben-Zvi, E. Zait, V. Dmitriev, E. Graitzer, G. Gottlieb, L. Leibovich, Pixer Technology (Israel); R. Birkner, K. Boehm, T. Scheruebl, Carl Zeiss SMS GmbH (Germany)

POSTER SESSION: ADVANCED RET

6730 4Y **Improvements in model-based assist feature placement algorithms** [6730-182]
B. Painter, L. D. Barnes, J. P. Mayhew, Y. Wang, Synopsys, Inc. (USA)

6730 4Z **An approach of auto-fix post OPC hot spots** [6730-183]
C.-H. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

6730 50 **3D mask modeling with oblique incidence and mask corner rounding effects for the 32nm node** [6730-184]
M. Saied, Freescale Semiconductor (France); F. Foussadier, STMicroelectronics (France); J. Belledent, NXP Semiconductors (France); Y. Trouiller, CEA/LETI (France); I. Schanen, IMEP (France); E. Yesilada, C. Gardin, Freescale Semiconductor (France); J. C. Urbani, F. Sundermann, F. Robert, STMicroelectronics (France); C. Couderc, NXP Semiconductors (France); F. Vautrin, STMicroelectronics (France); L. LeCam, NXP Semiconductors (France); G. Kerrien, J. Planchot, C. Martinelli, STMicroelectronics (France); B. Wilkinson, Freescale Semiconductor (France); Y. Rody, A. Borjon, NXP Semiconductors (France); N. Morgana, Freescale Semiconductor (France); J.-L. Di-Maria, CEA/LETI (France); V. Farys, STMicroelectronics (France)

6730 51 **Model-based mask verification** [6730-185]
F. Foussadier, F. Sundermann, STMicroelectronics (France); A. Vacca, J. Wiley, G. Chen, T. Takigawa, Brion Technologies, Inc. (USA); K. Hayano, S. Narukawa, S. Kawashima, H. Mohri, N. Hayashi, H. Miyashita, Dai Nippon Printing Co., Ltd. (Japan); Y. Trouiller, CEA/LETI (France); F. Robert, F. Vautrin, G. Kerrien, J. Planchot, C. Martinelli, STMicroelectronics (France); J.-L. Di-Maria, CEA/LETI (France); V. Farys, STMicroelectronics (France)

6730 52 **Inverse lithography technology (ILT): keep the balance between SRAF and MRC at 45 and 32 nm** [6730-212]
L. Pang, Y. Liu, T. Dam, K. Mihic, T. Cecil, D. Abrams, Luminescent Technologies, Inc. (USA)

POSTER SESSION: RET/OPC

6730 53 **More robust model built using SEM calibration** [6730-188]
C.-H. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

6730 54 **Safe interpolation distance for VT5 resist model** [6730-189]
W. Tawfic, M. Al-Imam, Mentor Graphics Corp. (Egypt); G. E. Bailey, Mentor Graphics Corp. (USA)

6730 55 **The effect of the OPC parameters on the performance of the OPC model** [6730-190]
A. Abdo, IBM Systems and Technology Group (USA); A. Seoud, Mentor Graphics Corp. (USA); A. Wei, I. Stobert, A. Leslie, IBM Systems and Technology Group (USA)

6730 56 **Modeling scanner signatures in the context of OPC** [6730-191]
Q. Zhang, Synopsys, Inc. (USA); J. K. Tyminski, Nikon Precision Inc. (USA); K. Lucas, Synopsys, Inc. (USA)

6730 57 **Modeling polarized illumination for OPC/RET** [6730-192]
H. Song, Q. Zhang, J. Shiely, Synopsys, Inc. (USA)

6730 58 **Fundamental study on the error factor for sub 90nm OPC modeling** [6730-193]
H. Lee, S.-U. Lee, J. Kim, K. Kim, DongbuHiTek (South Korea)

6730 59 **OPC development in action for advanced technology nodes** [6730-194]
A. C. Wang, Synopsys, Inc. (USA); M. Fujimoto, NEC Electronics Corp. (Japan); P. J. M. van Adrichem, I. Bork, Synopsys, Inc. (USA); H. Yamashita, NEC Electronics Corp. (Japan)

POSTER SESSION: MASK BUSINESS/MANAGEMENT

6730 5B **Industry survey of wafer fab reticle quality control strategies in the 90nm-45nm design-rule age** [6730-196]
R. Dover, KLA-Tencor Corp. (USA)

6730 5C **Shuttle fabrication for designs with lifted I/Os** [6730-197]
R.-B. Lin, M.-C. Wu, S.-L. Tsai, Yuan Ze Univ. (Taiwan)

POSTER SESSION: EUV AND OTHER GENERATION LITHOGRAPHY

6730 5D **Development status of EUVL mask blanks in AGC** [6730-198]
K. Hayashi, Asahi Glass Co., Ltd. (Japan)

6730 5E **Performance of actinic EUVL mask imaging using a zoneplate microscope** [6730-199]
K. A. Goldberg, P. P. Naulleau, Lawrence Berkeley National Lab. (USA); A. Barty, Lawrence Livermore National Lab. (USA); S. B. Rekawa, C. D. Kemp, R. F. Gunion, F. Salmassi, E. M. Gullikson, E. H. Anderson, Lawrence Berkeley National Lab. (USA); H.-S. Han, SEMATECH (USA)

6730 5F **The effect of size and shape of sub-50 nm defects on their detectability** [6730-200]
A. Rastegar, W. Cho, SEMATECH (USA); E. Gullikson, Lawrence Berkeley National Lab. (USA); S. Eichenlaub, SEMATECH (USA)

6730 5G **Techniques to measure force uniformity of electrostatic chucks for EUV mask clamping** [6730-201]
S. Veeraraghavan, J. Sohn, K. T. Turner, Univ. of Wisconsin, Madison (USA)

6730 5H **A study of precision performance and scan damage of EUV masks with the LWM9000 SEM** [6730-202]
I. Yonekura, H. Hakii, T. Yoshii, Y. Negishi, K. Oohira, K. Kanayama, M. Kawashita, Y. Sakata, K. Tanaka, Toppan Printing Co., Ltd. (Japan)

6730 5I **EUV mask substrate flatness improvement by laser irradiation** [6730-203]
K. Takehisa, J. Kodama, H. Kusunose, Lasertec Corp. (Japan)

6730 5J **Evaluation of EUVL-mask pattern defect inspection using 199-nm inspection optics** [6730-204]
T. Amano, Y. Nishiyama, H. Shigemura, T. Terasawa, O. Suga, MIRAI-Semiconductor Leading Edge Technologies, Inc. (Japan); H. Hashimoto, N. Kameya, NuFlare Technology, Inc. (Japan); S. Murakami, N. Kikuiri, Advanced Mask Inspection Technology Inc. (Japan)

6730 5K **Study of impacts of mask structure on hole pattern in EUVL** [6730-205]
N. Iriki, Y. Arisawa, H. Aoyama, T. Tanaka, Semiconductor Leading Edge Technologies Inc. (Japan)

6730 5L **Repair specification study for half-pitch 32-nm patterns for EUVL** [6730-206]
H. Aoyama, T. Amano, Y. Nishiyama, H. Shigemura, O. Suga, MIRAI-Semiconductor Leading Edge Technologies, Inc. (Japan)

6730 5M **EUV mask process development using DUV inspection system** [6730-207]
D. Kim, V. Vellanki, W. Huang, A. Cao, C. Chen, A. Dayal, P. Yu, K. Park, Y. Maenaka, K. Jochi, G. Inderhees, KLA-Tencor Corp. (USA)

6730 5N **Development of EUV mask fabrication process using Ru capping blank** [6730-208]
T. Abe, T. Adachi, S. Sasaki, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); K. Ishikiriyama, Intel Corp. (Japan)

POSTER SESSION: IMPRINT

6730 5O **Metrology for templates of UV nano imprint lithography** [6730-209]
K. Yoshida, K. Kojima, M. Abe, S. Sasaki, M. Kurihara, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

6730 5P **UV-NIL template for the 22nm node and beyond** [6730-210]
T. Hiraka, S. Yusa, A. Fujii, S. Sasaki, K. Itoh, N. Toyama, M. Kurihara, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

6730 5Q **A study of template cleaning for nano-imprint lithography** [6730-211]
J. E. Ellenson, L. C. Litt, A. Rastegar, SEMATECH (USA)

Author Index

Conference Committee

Conference Chairs

Robert J. Naber, Cadence Design Systems, Inc. (USA)
Hiroichi Kawahira, Sony Corporation (Japan)

Program Committee

Ki-Ho Baik, Intel Corporation (USA)
Artur P. Balasinski, Cypress Semiconductor Corporation (USA)
Uwe F. W. Behringer, UBC Microelectronics (Germany)
Robert M. Bigwood, Intel Corporation (USA)
Ron R. Bozak, RAVE LLC (USA)
William H. Broadbent, KLA-Tencor Corporation (USA)
Peter D. Buck, Toppan Photomasks, Inc. (USA)
Jang Fung Chen, ASML MaskTools Inc. (USA)
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)
Frank A. J. M. Driessen, Takumi Technology B.V. (Netherlands)
Roxann L. Engelstad, University of Wisconsin, Madison (USA)
Benjamin G. Eynon, Jr., SAMSUNG (USA)
Donis G. Flagello, ASML US, Inc. (USA)
Emily E. Gallagher, IBM Microelectronics Division (USA)
Bernd Geh, Carl Zeiss / ASML-TDC (USA)
Brian J. Grenon, Grenon Consulting, Inc. (USA)
Woo-Sung Han, SAMSUNG Electronics Company, Ltd. (South Korea)
Naoya Hayashi, Dai Nippon Printing Company, Ltd. (Japan)
Alan J. Leslie, IBM Corporation (USA)
Chin-Hsiang Lin, Taiwan Semiconductor Manufacturing Company, Ltd. (Taiwan)
Paul F. Luehrmann, Jr., ASML Netherlands B.V. (Netherlands)
Patrick M. Martin, Photronics, Inc. (USA)
Mark E. Mason, Texas Instruments Inc. (USA)
Wilhelm Maurer, Infineon Technologies AG (Germany)
Warren M.Montgomery, Albany NanoTech (USA)
Richard D. Morse, Silicon Canvas Inc. (USA)
Thomas H. Newman, Micronic Laser Systems AB (USA)
Steven D. Slonaker, Nikon Precision Inc. (USA)
Christopher A. Spence, AMD Saxony LLC & Company KG (Germany)
Wolfgang Staud, B^{2}W Consulting (USA)
Geert Vandenberghe, IMEC (Belgium)
J. Tracy Weed, Synopsys, Inc. (USA)
Craig A. West, Toppan Photomasks, Inc. (USA)
Vincent Wiaux, IMEC (Belgium)

Session Chairs

1 Invited Session
Robert J. Naber, Cadence Design Systems, Inc. (USA)
Hiroichi Kawahira, Sony Corporation (Japan)

2 Etch
Ki-Ho Baik, Intel Corporation (USA)
Warren M. Montgomery, Albany NanoTech (USA)

3 Substrate
Uwe F. W. Behringer, UBC Microelectronics (Germany)
Roxann L. Engelstad, University of Wisconsin, Madison (USA)
Benjamin G. Eynon, Jr., SAMSUNG (USA)

4 Imprint
Naoya Hayashi, Dai Nippon Printing Company, Ltd. (Japan)
Ron R. Bozak, RAVE LLC (USA)
Bernd Geh, ASML US, Inc. (USA)

5 Resist
Ki-Ho Baik, Intel Corporation (USA)
Peter D. Buck, Toppan Photomasks, Inc. (USA)
Warren M. Montgomery, Albany NanoTech (USA)

6 DFM 1: Masks and Manufacturability
Robert M. Bigwood, Intel Corporation (USA)
Artur P. Balasinski, Cypress Semiconductor Corporation (USA)
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)

7 DFM 2: Manufacturing Models and Physical Design
Robert M. Bigwood, Intel Corporation (USA)
Mark E. Mason, Texas Instruments Inc. (USA)
Wilhelm Maurer, Infineon Technologies AG (Germany)

8 DFM 3: Modal Aware Design and Optimization
Artur P. Balasinski, Cypress Semiconductor Corporation (USA)
Richard D. Morse, Silicon Canvas Inc. (USA)
Frank A. J. M. Driessen, Takumi Technology B.V. (Netherlands)

9 EUV and OGL
William H. Broadbent, KLA-Tencor Corporation (USA)
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)
Warren M. Montgomery, Albany NanoTech (USA)

10 Cleaning I
Naoya Hayashi, Dai Nippon Printing Company, Ltd. (Japan)
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)
Byung Cheol Cha, SAMSUNG Electronics Company, Ltd. (South Korea)

11 Cleaning II
Naoya Hayashi, Dai Nippon Printing Company, Ltd. (Japan)
Brian J. Grenon, Grenon Consulting, Inc. (USA)
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)

12 Extreme NA
Donis G. Flagello, ASML US, Inc. (USA)
Thomas H. Newman, Micronic Laser Systems Inc. (USA)
Geert Vandenberghe, IMEC (Belgium)

13 Simulation
Bernd Geh, ASML US, Inc. (USA)
Frank A. J. M. Driessen, Takumi Technology B.V. (Netherlands)
Roxann L. Engelstad, University of Wisconsin, Madison (USA)

14 Repair I
Benjamin G. Eynon, Jr., SAMSUNG (USA)
J. Tracy Weed, Synopsys, Inc. (USA)

15 Repair II
Benjamin G. Eynon, Jr., SAMSUNG (USA)
J. Tracy Weed, Synopsys, Inc. (USA)

16 Inspection
William H. Broadbent, KLA-Tencor Corporation (USA)
Emily E. Gallagher, IBM Corporation (USA)
Craig A. West, Toppan Photomasks, Inc. (USA)

17 Advanced RET
Wilhelm Maurer, Infineon Technologies AG (Germany)
Brian J. Grenon, Grenon Consulting, Inc. (USA)
Alan J. Leslie, IBM Corporation (USA)

18 RET I
Wolfgang Staud, B^{2}W Consulting (USA)
Christopher A. Spence, Advanced Micro Devices, Inc. (USA)
Peter D. Buck, Toppan Photomasks, Inc. (USA)

19 RET II
Wolfgang Staud, B^{2}W Consulting (USA)
Christopher A. Spence, Advanced Micro Devices, Inc. (USA)
Peter D. Buck, Toppan Photomasks, Inc. (USA)

20 Mask Business/Management
Han-Ku Cho, SAMSUNG Electronics Company, Ltd. (South Korea)
Mark E. Mason, Texas Instruments Inc. (USA)

21 Patterning
Peter D. Buck, Toppan Photomasks, Inc. (USA)
Thomas H. Newman, Micronic Laser Systems Inc. (USA)
Patrick M. Martin, Photronics, Inc. (USA)

22 Metrology I
Thomas H. Newman, Micronic Laser Systems Inc. (USA)
Bernd Geh, ASML US, Inc. (USA)
Emily E. Gallagher, IBM Corporation (USA)

23 Metrology II
Thomas H. Newman, Micronic Laser Systems Inc. (USA)
Bernd Geh, ASML US, Inc. (USA)
Emily E. Gallagher, IBM Corporation (USA)

24 MDP
Richard D. Morse, Silicon Canvas Inc. (USA)
Artur P. Balasinski, Cypress Semiconductor Corporation (USA)
Patrick M. Martin, Photronics, Inc. (USA)

Poster Sessions
Wolfgang Staud, B_2W Consulting (USA)
Hiroichi Kawahira, Sony Corporation (Japan)

Introduction

This proceedings volume contains accepted papers from the SPIE conference on Photomask Technology. The conference was arranged through the Bay Area Chrome Users Society (BACUS) and held as part of the 27th International Symposium on Photomask Technology 18–21 September 2007 in Monterey, California, USA.

The papers contained in these proceedings cover the latest advances in photomask technology. In addition, components that influence the photomask industry such as lithography approach, design, and resolution enhancement as well as the emerging technology are captured within the scope of influencing photomask technology going forward. Business aspects that examine cost-friendly and manufacturable solutions for our industry are reviewed as well.

This year's symposium continued the fine tradition of having wide international representation with a record number of papers divided into the following categories;

- Mask Infrastructure
    - Materials
    - Patterning
    - Resist Processing
    - Etch
    - Clean
    - Inspection
    - Repair
    - Metrology
- Mask Integration
    - Design For Manufacturing/Process Integration
    - Simulation and Mask Tolerance for Hyper NA
    - Extreme NA Imaging Effects
    - Reticle Enhancement and Proximity Effects
    - Mask Data Preparation and Mask Rules
- Emerging Mask Technology
    - Extreme UV Impact
    - Imprint
    - Gray Scale
- Mask Business
    - Cost and performance
    - Multi Project Masks
    - Direct Write or Maskless Technology.

This year's special session with industry experts from around the world spanning design (IDM and fabless), maskmaking (Captive and Merchant), and wafer manufacturing (IDM and Foundry) met to explore the topic: "Double Patterning Lithography: Challenges and Approaches to Implementation—Twice the Pain for Twice the Gain." The program listing of participants, a summary by Marc Levenson, and a link to the presentations online are available in the pages following this introduction.

I thank the authors, particularly the keynote speaker Rick Wallace, CEO of KLA-Tencor, speaking on the "Collaboration, Innovation, and Execution: Three Keys to Premium Customer Experience."

I also thank members of the program committee for their dedication and hard work to help maintain the high quality of this conference. I am also grateful to my co-chair Hiroichi Kawahira for all his help in making this year's symposium a success. Of course, the sponsors who allow us to continue to attract talented speakers deserve recognition for without them, we would not be able to exist as a conference. Finally, I extend my sincere appreciation to the SPIE staff for their tireless efforts and their meticulous organizational skills that helped make this year's SPIE Photomask Technology conference a success, including a special thank you to SPIE for assembling and publishing this proceedings volume.

I hope you find the material comprehensive and valuable to your technical field, whatever that may be. BACUS is a professional society. If you are interested in what we are about, please visit the technical group on the SPIE website at www.SPIE.org/BACUSHome and join us as we continue to influence photomask technology development through our respected career applications.

Robert J. "Bob" Naber
Cadence Design Systems, Inc.

Friday Special Session Schedule

Double Patterning Lithography: Challenges and Approaches to Implementation—Twice the Pain for Twice the Gain *

Chairs: **Hiroichi Kawahira,** Sony Corporation (Japan); **Artur P. Balasinski,** Cypress Semiconductor Corporation; **Jo M. Finders,** ASML Netherlands B.V. (Netherlands)

Introduction

Summary of BACUS Panel Discussion on ITRS-DPL at Advanced Lithography (2007)
Artur P. Balasinski, Cypress Semiconductor Corporation

Lithography Perspectives

Donald Samuels, IBM Corporation (USA)

Robert M. Bigwood, Intel Corporation (USA)

Luigi Capodieci, Advanced Micro Devices, Inc. (USA)

Steven R. J. Brueck, CHTM/The Univ. of New Mexico (USA)

Mircea V. Dusa, ASML US, Inc. (USA)

Ivan Lalovic, Cymer, Inc. (USA)

Mireille Meanhoudt, IMEC (Belgium)

EDA Perspectives

Judith A. Huckabay, Cadence Design Systems, Inc. (USA)

Frank M. Schellenberg, Mentor Graphics Corporation (USA)

Mask Perspectives

Takashi Kamikubo, NuFlare Technology, Inc. (Japan)

William H. Broadbent, KLA-Tencor Corporation (USA)

Jun Wei Bao, Timbre Technologies, Inc. (USA)

Han-ku Cho, SAMSUNG Electronics Co., Ltd. (South Korea)

Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

Franklin D. Kalk, Toppan Photomasks, Inc. (USA)

Closing Remarks

---

* For materials relating to this session point your web browser to: www.SPIE.org/PM07
* For information about the BACUS technical group go to: www.SPIE.org/BACUSHome

Summary of the Friday Special Session

Doubling down at BACUS*

Double patterning technology (DPT), self-aligned or not, seemed to be the consensus choice for the next half-pitch node or two for the maskmakers convened in Monterey for SPIE's annual BACUS Symposium on Photomask Technology (Sept. 16–21) — not that anyone thought it would be easy. The evident delay in EUV technology poses special challenges for the photomask community and these were highlighted in a special Friday session, sub-titled: "Twice the pain for twice the gain."

Artur Balaskinki of Cypress Semiconductor began the session by reviewing the results from the SPIE panel held in February: Double exposure double etch (DEDE) methods (where the pattern of one resist film is developed and transferred before a second film is applied, etc.) are expected to get to k_1=0.18, which corresponds to 26nm half-pitch with water immersion. Self-aligned spacer/trim (SAS/T) methods (where a deposition step coats a sacrificial spacer pattern with a hard mask, subsequently trimmed, etc.) are projected to approach k_1=0.13 (19nm hp), both well below the single-resist k_1=0.25 limit. In spite of the evident difficulties — litho CDU specs below 3.5% and overlay at 7% for DEDE but up to 20% for SAS/T, etc. — February's expert panel predicted that the NAND manufacturers (at least) would do it.

Don Samuels of IBM introduced the litho-user's perspective by countering that DPT was a last resort, being developed in IBM alliances for prototyping, but not necessarily for production. However, the very restricted design rules required for a product to be built using DPT pointed toward improved yield with less exotic techniques. Methods devised for alternating phase shift mask designs were being re-applied.

Robert Bigwood of Intel observed that the DfM strategies that had to be implemented for DPT were not disruptive and need not lead to a great increase in time-to-silicon, especially if tasks were done in parallel. However, the mask data prep volume was going to be larger. Luigi Capodieci of AMD noted that there was a trade-off between process complexity and material sophistication. For example, a practical nonlinear resist or CEL could make the second coat and etch steps of DEDE unnecessary. Even so, materials companies are not actively seeking materials that would facilitate DPT, even simple ones like negative 193nm resist.

Mircea Dusa of ASML pointed out that DPT would be a challenge to the entire production system, not just lithography. In particular, etch bias would be a major CDU contributor and metrology needed to be improved — quickly. He suggested

that metrology tools could be used for compensation, not just dispositioning, so that anomalies like a reticle CD fingerprint on one exposure could be compensated in the second using a pre-distorted dose profile, for one example. Dedicated tools might be needed, though, both for exposure and metrology, ending "mix-and-match."

Dusa also presented a paper from Mireille Maenhoudt of IMEC that sketched numerous double patterning options, from "freezing" the first resist pattern (thereby reducing the number of hard masks needed) to double development, where the highly exposed regions of resist dissolve in a positive-tone developer while unexposed regions are removed in a negative-tone developer, leaving a grating with half the exposed pitch. It remains to be proved that all the CDs can be controlled sufficiently to yield working circuits, but the proof-of-principle experiments have been done, he said.

Speakers from EDA companies Cadence and Mentor Graphics emphasized that DPT litho tools must be embedded in today's designer flows, without disruption — fabless companies are fabless because they don't want to know manufacturing details, even crucial ones. Nevertheless, there is a successful example of design interfacing with sophisticated manufacturing models: RET.

Maskmakers and tool vendors seemed remarkably sanguine about DPT, perhaps because of the possibility for increasing volume. Takihashi Kamikubo of Nuflare, the dominant manufacturer of e-beam write tools, pointed out that scanner alignment errors dominated mask effects. The low stress mask blanks and charge dissipation layers thought to be needed to meet the demands of double patterning already exist. Bill Broadbent of KLA-Tencor claimed that their 600 series defect detection tools would meet the "basic requirements" of 32nm DPT masks in 2009. However, he did note that the company offers no placement metrology tools, and the 600 would not detect the displacement of an entire region of a plate. Jun Wei Bao of Timbre Technologies suggested that a scatterometry-based method would soon achieve sufficient overlay and CD sensitivity for 32nm DPT.

Han-Ku Cho described the present state of the art of DPT achieved by Samsung, which does not expect any other litho solutions to be available by 2009. He pointed out that the scanner stage randomness consumed 60% of the error budget in DEDE DPT, motivating SAS/T techniques, and asked for accelerated development of an image placement metrology tool sufficient to fulfill the DPT registration specs.

Images of hamburgers with one, two, and four patties were served up by DNP Fellow Naoya Hayashi to illustrate the challenges of multiple patterning lithography. Overlay becomes more challenging as the number increases, but DfM restrictions are reduced because more geometries can be separated without conflict when the mask set is larger. Because of manufacturing efficiencies and quality trade-offs, the cost of a DPT mask set would only be 1.7X

that of a comparable single mask, not 2X — just as a double hamburger does not cost twice as much as a single patty, he explained.

Franklin Kalk of Toppan Photomasks concluded the usually dour mask-making symposium with a remarkably optimistic view: It is all do-able! He claimed that the "random" placement errors characteristic of certain e-beam mask writing tools are not random at all, but correctable systematics related to the position of the beam in the physical lens aperture, which is not presently modeled or measured. So while tool development is necessary, it is not impossible to understand and correct the errors with the most impact. In addition, when 32nm logic actually has a minimum pitch of 90nm, Kalk claimed it is possible to meet the 5nm overlay spec by selecting the best masks from current production. Even a 1nm CD spec is doable if all of the improvements that maskmakers know about — but have found uneconomical to apply — are actually implemented, he predicted. Kalk also mentioned that he had just recovered from the bite of a mysterious spider and was looking forward to new adventures.

M. David Levenson

---

* Reprinted from the October edition of *WaferNews.* Copyright 2007 by PennWell.

View other articles from *Microlithography World* at: www.microlithographyworld.com.