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C. Sellier

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CMOS Microcamera for Space Applications (3DCM681)

C. Sellier[1], D. Gambart[1], N. Perrot[1], E. Garcia-Sanchez[1], C. Virmontois[2] and A. Bardoux[2]

[1]3D PLUS, Buc, France, *csellier@3d-plus.com*

[2]Centre National d'Etudes Spatiales (CNES), Toulouse, France

I. INTRODUCTION

3D PLUS has developed in the framework of R&D activities an advanced CMOS camera for Space applications. The Centre National d'Etudes Spatiales (CNES), also called French space agency, is leading the developement of this camera, see Figure 1. This instrument has been integrated using the 3D PLUS technology in order to be as compact as possible. Particular attention has been paid to ensure a good radiation tolerance to cover a wide range of scientific applications such as planetology, but also platform or launcher monitoring and star trackers.

Figure 1: Microcamera bottom and side views

II. ARCHITECTURE

The 3DCM681 microcamera is made of a 4Mpixels CMOS image sensor (same as CIS1 defined in [1]), a FPGA for interfacing the image sensor with the instrument system, an oscillator, volatile and non-volatile memories, biasing and protection circuits.

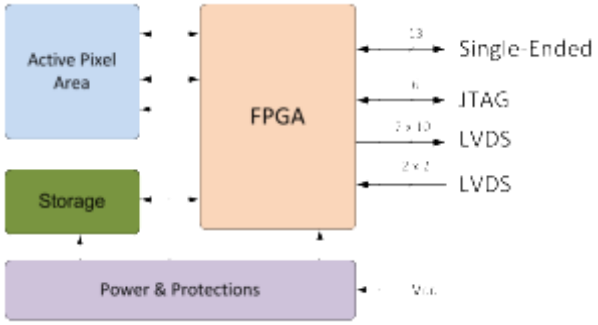

Figure 2: Functional architecture of the microcamera

The CMOS sensor is constituted by 2048 x 2048, 5.5µm-pitch pixels. Each pixel is based on pinned photodiode architecture with several transistors. This sensor is fully digital, it contains an on-chip microcontroller, registers, per column ADCs (2048) and can be read using 16 Low Voltage Differential Signaling (LVDS) outputs. The behavior of the digital part of the sensor against Single Event Effects (SEE) has been evaluated by CNES and shows low upset events and the need for a protection against Single Event Latchup (SEL). Red, green and blue color filters are introduced in the optical stack above each pixel using a Bayer array distribution. Microlenses are deposited on the top of each pixel at the end of the image sensor process. This optical element focuses the incident light in the pixel to improve the pixel quantum efficiency.

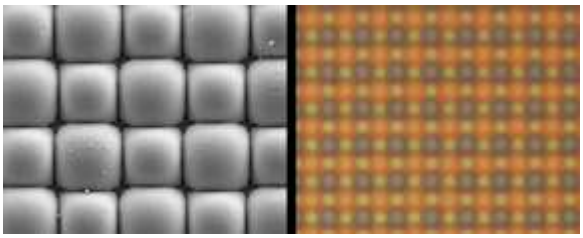

Figure 3: SEM images of the Microlense (left) and optical image of the color filter array (right). Microlenses are single layer polymer and less than 1µm thickness. Pixel pitch is 5.5µm.

The Field Programmable Gate Array (FPGA) has a 3.000.000 system gates capacity and uses a low power technology, latchup free and radiation tolerant up to 30krads. It is used for smart interface between image sensor, memory and external system with the ability to perform preliminary image processing as averaging, adding, windowing etc… A serial interface is used to sending commands to the camera, LVDS interface is used for camera output. FPGA can be suited by the user to the system needs by modifying its programmation code. An oscillator provides the clock signal to the FPGA.

A 1G x 8bits non-volatile flash NAND memory is used to store reference pictures or cartography.

A 128M x 8bits volatile SDRAM memory is used for image storing or processing.

Four different voltages (3.3V, 2.5V, 2.1V and 1.5V) necessary for supplying the sensor, the oscillator, the FPGA and the memories are internally generated from a single VIN supply voltage by using voltage regulators. The input supply voltage VIN of the microcamera module shall be between 4.5V and 9V.

Protection circuit against SEL is integrated in the camera since the CMOS sensor is sensitive to Single Event Latchup. Its principle is based on overcurrent detection able to send a warning information to the FPGA. When the FPGA receives this signal, supply voltages of the CMOS sensor are switched off and the FPGA buffers interfacing with the CMOS sensor are set to high impedance state (in order to avoid sensor biasing through interface signals). This protection circuit is implemented for each sensor supply voltage.

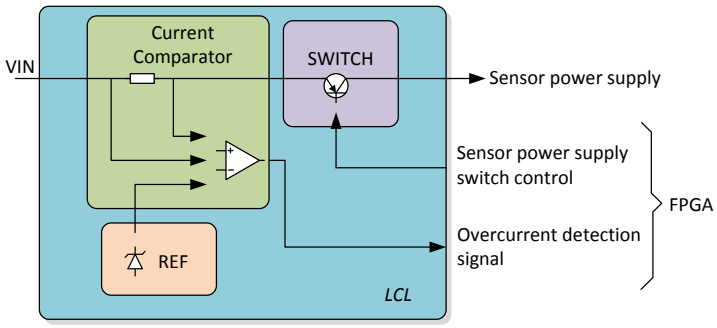

Figure 4: Principle of protection circuit against SEL

The detailed electrical architecture of the CMOS microcamera module is shown hereafter :

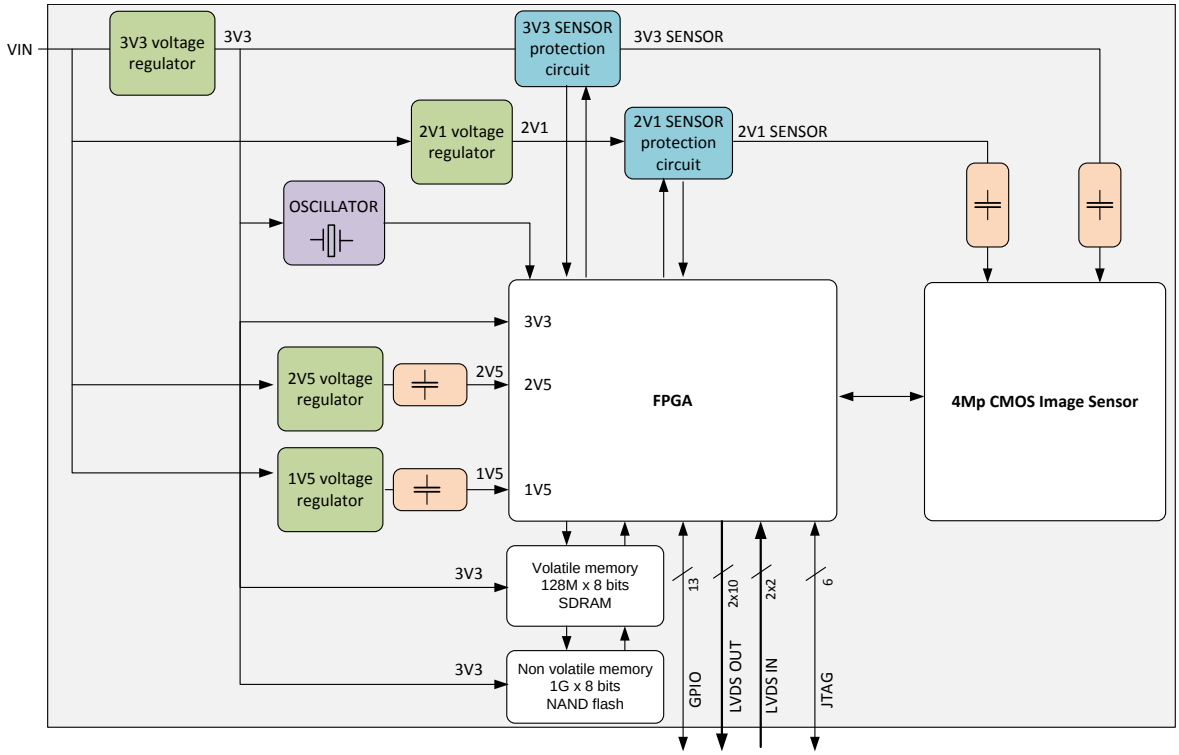

Figure 5: Electrical architecture of the microcamera

III. USE AND ADVANTAGES OF 3D PLUS STACKING TECHNOLOGY

The 3DCM681 microcamera has been designed and manufactured with 3D PLUS stacking technology. This 3D technology is based on the stacking of electronic components (chips, plastic packages, sensors) reported on a thin pcbs, and so called flex. This solutions allows testing and screening the components of each layer before stacking. This is the key feature for building 'n'-High stacks with a very good yield. The flex are then stacked vertically and connected together thanks to a vertical interconnection technique.

This System-In-Packages (SiPs) technology allows gaining a factor of at least 10 on weight and volume of the components. It enables achieving a combination that cannot be realized with monolithic System-

on-Chip (SoC) approaches. This capability domain is referenced as FLOW 2 and is qualified by European Space Agency (ESA) for Space applications.

The manufacturing process is shown in **Erreur ! Source du renvoi introuvable.**.

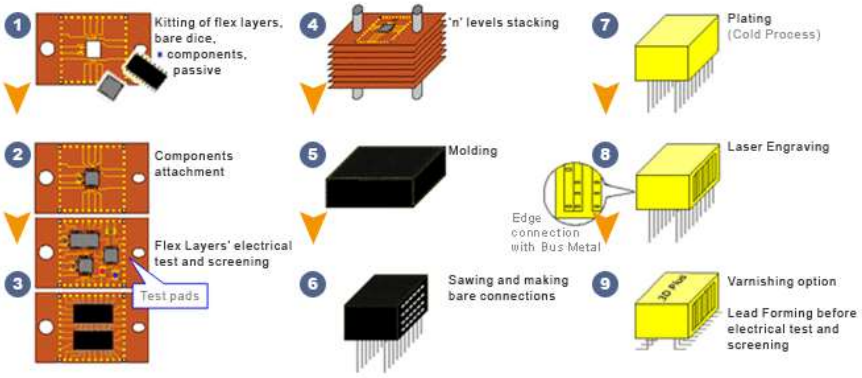

Figure 6: 3D PLUS stacking technology manufacturing process

The 3DCM681 microcamera includes 4 stacked levels in order to obtain a 3D cube with a reduced volume of 35x35x25 mm^3.

The bottom of the camera contains a PGA array where a flex can be connected to insure the link to the system. The PGA array is able to cover a wide range of connections, from standard LVDS to SpaceWire depending on the FPGA code. The second level contains power supplies, the oscillator and the non volatile memory. The third level includes the FPGA and the volatile memory. The top level contains the 2048x2048 pixels color CMOS image sensor which is the key element of the camera. It also includes the protection circuitry of the image sensor.

The 3D module in its prototype version is available now, electrical and electro optical characterizations are in progress. Microcamera modules dedicated for space applications will be manufactured and qualified by the end of year 2016.

IV. CAMERA PERFORMANCES

The camera can be used up to 16 frames per second in 10-bits pixel mode (up to 12 frames/s in 12-bits pixel mode).
Thanks to the embedded fast volatile memory we are able to perform picture treatment like RGB binning, averaging, subsampling, windowing.

ACKNOWLEDGEMENTS

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