Semiconductor Design for Tuned Charge Transport Characteristics

Antonio Facchetti*[a], Zhihua Chen [a], Yen Zheng [a], Jordan R. Quinn [a], Christopher R. Newman [a], He Yan [a], Tse Nga Ng,* [b] Sanjiv Sambandan [b], Rene Lujan [b] and Ana Claudia Arias [b]

[a] Polyera Corporation, 8045 Lamon Avenue, Suite 140, Skokie, IL 60077, USA
[b] Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304, USA

ABSTRACT

In this paper we report on the use of two solution-processable polymeric and molecular n-channel semiconductors for the fabrication of transistors and CMOS inverters by gravure printing and inkjet printing. Furthermore, the injket-printed TFT/invertor stability characteristics are analyzed and discussed.

Keywords: TFT, transistor, organic semiconductor, printing, bias stress,

1. INTRODUCTION

The integration of hole-transporting (p-channel) and electron-transporting (n-channel) thin-film transistors (TFTs) in the same device architecture to enable complementary circuit technologies is one of the most powerful routes to enhance speed and reliability of electronic circuits.[1] Organic semiconductors are viewed as alternative active materials to conventional silicon-based electronics, possibly enabling a new generation of inexpensive, low-temperature processed, and mechanically flexible devices for display, sensor, and memory applications.[2] Because organic semiconductor performance is typically lower than that of inorganic materials, the successful integration of p- and n-channel organic thin-film transistors (OTFTs) is even more important. As far as organic complementary circuits are concerned, there are two key requisites to be satisfied for inexpensive device fabrication. First, it is essential that both p- and n-channel semiconductors are solution-processable and operationally stable in ambient conditions. While several p-channel organic semiconductors have achieved high mobility (~1-5 cm2/Vs) and are commercially available, their n-channel counterparts have traditionally shown lower performance and stability. Recent efforts on improving n-channel TFTs have been fruitful, leading to commercially available air-stable n-channel materials with mobility ~1-2 cm2/Vs for vapor-deposited semiconductor films[3] and ~0.5-1 cm2/V s for solution-processed films.[4] These materials may enable the fabrication of organic complementary circuits which have the advantages of lower power consumption and simpler design compared to unipolar circuits. Second, it is desirable to avoid expensive photolithographic processes to define the critical source-drain TFT channel region and to pattern the p- and n-channel semiconductors. To this end, inkjet printing is a viable approach for depositing/patterning contact materials with resolution in the micrometer regimes.[5]

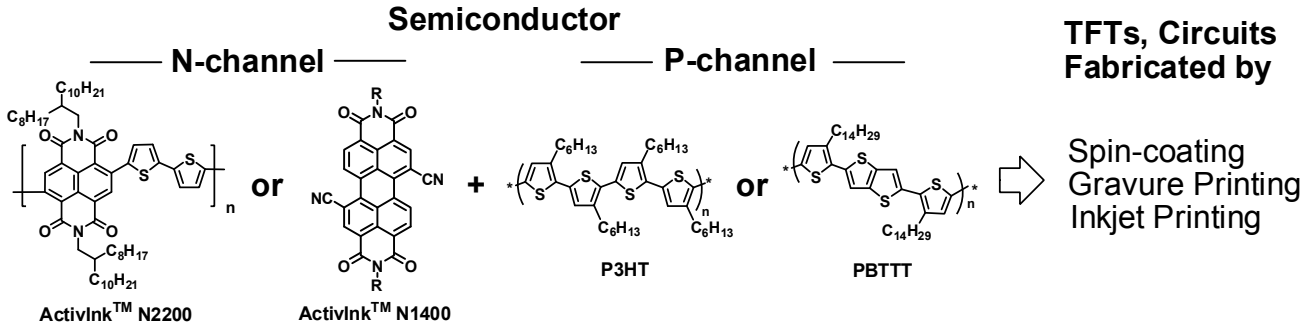

Figure 1. Semiconductors used in this study.

*: afacchetti@polyera.com; phone 1 847 6777570; fax 1 847 677757510

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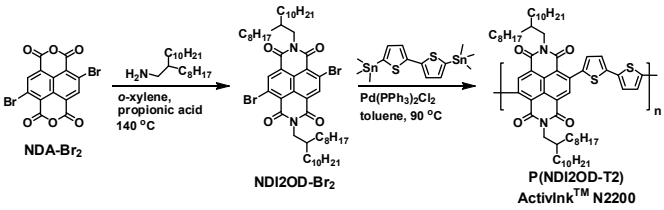
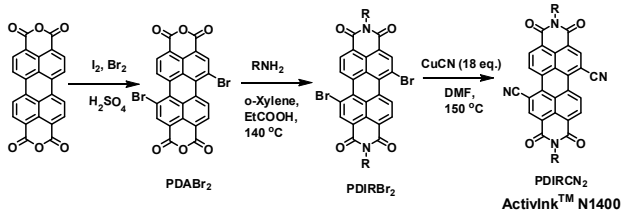
In this paper we reeport on the implementation of soluble rylene-based molecular and polymeric n-channel semiconductors (ActivInk N1400 and N2200, respectively) with p-channel materials (P3HT and PBTTT) aand a common dielectric/contact materials set to fabricate gravure- and inkjet-printed TFTs and complementary inverters in ambient conditions (Fig. 1). Furthermore, for the inkjet-printed devices, the bias stress effects of these TFTs and the dc and ac responses of the corresponding inverters are presented. The threshold-voltage shifts between p- and n-type TFTs are examined to estimate the inverter noise margins after electrical bias stress.

2. N-CHANNEL SEMICONDUCTOR SYNTHESIS

Two Polyera n-channel materials were used in this study. The first is a naphthalene-based polymer (ActivInk D2200) which has been synthesized according to Scheme 1.



Scheme 1. Synthesis of ActivInk N2200.



Scheme 2. Synthesis of ActivInk N1400.

The perylene-based molecular semiconductor (ActivInk D1400) has been synthesized according to Scheme 2. Both materials have been characterized by conventional analytical methods and their purity accessed by NMR and EA. Importantly, the electronic structure of both semiconductors, characterized by LUMO energies < - 4 eV, is compatible with ambient-stable electron transport.

3. GRAVURE-PRINTED TFTS AND CIRCUITS USING ACTIVINK N2200 AND P3HT

The top-gate bottom-contact (TGBC) TFT structures used in this part of the study are the following: glass(substrate)/Au(source-drain contacts)/ ActivInk N2200 /ActivInk D2200 (dielectric) /Au(gate contact) and PET(substrate)/Au/ActivInk N2200/ActivInk D2200/Au. The TGBC structures were fabricated with the ACTIVINK N2200 film deposited by spin-coating and gravure printing the semiconductor and spin-coating the dielectric. Furthermore, all-gravure-printed devices were fabricated. All device fabrication processes were performed in ambient conditions with the exception of the Au contact vapour deposition and the film drying steps (≤ 110 ºC).

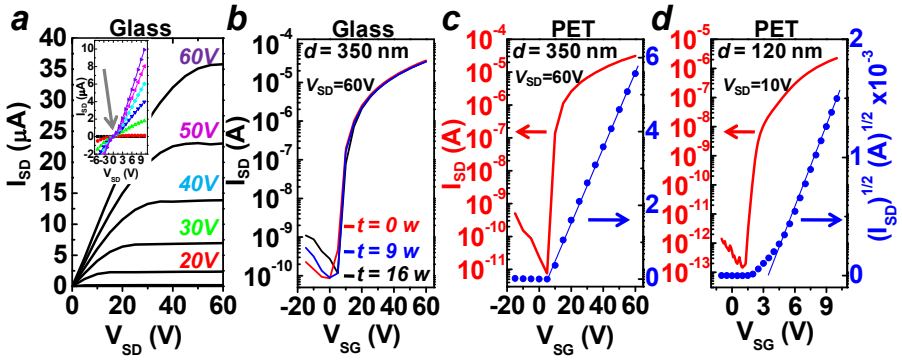


Figure 2. Performance and stability in ambient of representative TFT devices with spin-coated ActivInk N2200 semiconductor and ActivInkTM D2200 (of thickness d) layers. a. Current-voltage output plot as a function of V_{SG} for a representative TGBC device on glass. Inset: Low-voltage scan highlighting the linear I-V characteristics and the line intersection through the axes origin. b. TFT transfer plots of current vs. V_{SG} for a representative TGBC device on glass measured immediately after fabrication (black) and 9 (red) and 16 (blue) weeks after fabrication. c. TFT transfer plot of current vs. V_{SG} for a representative TGBC device on PET. d. TFT transfer plot of current vs. V_{SG} for a representative TGBC device on PET with a ~120 nm-thick dielectric layer.

Figure 2 shows representative output (Fig. 2a) and transfer (Fig. 2b) current-voltage plots for a TGBC TFTs fabricated by spin-coating both the semiconductor and the dielectric layers on glass/Au substrates. The analysis of the output plot at low V_{SD} (Fig. 2a Inset) reveals excellent electron injection from high workfunction Au contacts with no significant sub-linear characteristics. These devices exhibit very high performance, with average μ_e's ~ 0.5 cm2/Vs, I_{on}:I_{off} ~ 10^7, V_{on} ~ +3 V, V_{th} ~+7 V, and S < 2 V/dec with yields approaching 100%. Several devices from different batches exhibit μe's ~ 0.85 cm^2/Vs with Ion:Ioff > 10^6. Note that statistically comparable device performance and device yields were achieved for TGBC TFTs on PET plastic substrates (Fig. 2c). Furthermore, thanks to the optimized semiconductor film morphology and the quality of our dielectric material, TGBC TFTs based on a very thin spin-coated dielectric layer (<200 nm) were fabricated for the first time (Fig. 2d). The resulting TFTs operate at < 10 V and achieve S as low as ~280 mV/dec.

Gravure-printing of ActivInk N2200 solutions was optimized by controlling semiconductor concentration and solvent mixtures (1-2% w/w in DCB-CHCs), printing speed and force, and number of passes of the gravure cylinder on the PET/Au(source-drain contacts) substrates. For successful TFT fabrication by printing it is necessary to achieve a smooth and uniform semiconductor film morphology as well as complete substrate coverage so that a pinhole-free gate dielectric film can be deposited on top. Furthermore, an interesting question is whether a thin gate dielectric layer can be utilized for TFT fabrication with a printed semiconductor. This is relevant for low-voltage TFT operation.

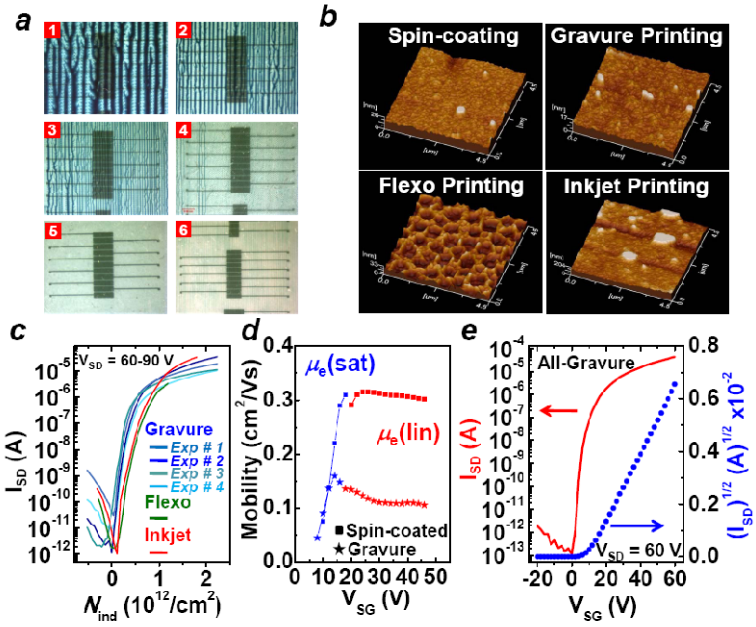


Figure 3. ActivInk N2200 film morphologies and TGBC TFT performance for polymer films/devices fabricated using various solution-processing techniques on PET/Au substrates. a. Optical images of ActivInk N2200 films with underlying Au source-drain contacts gravure-printed from a 2% w/w polymer DCB-CHC solution and using printing disks with decreased gravure cell depth(μm)/volume(mL/m2) (cell D/V). Image #1 (D/V=80/23.3), #2 (D/V=65/15.6), #3 (D/V=45/6.1), #4 (D/V=40/8.8), #5 (D/V=30/4.1), #-6 (D/V=10/0.5). The optimized film morphology corresponds to image #5. b. Atomic force microscopy (AFM) images of spin-coated and printed films c. Representative TFT transfer plots of current vs. carrier density (Nind) of various gravure-printed TGBC TFTs with dielectric and semiconductor layers of different thicknesses. d. TFT transfer plots of current vs. VSG for a representative flexo-printed (red) and inkjet-printed (blue) TGBC device. e. TFT transfer plot of current vs. VSG for a representative fully gravure-printed TGBC device.

Figure 3a (panels 1 to 6) provides an example of gravure-printing optimization, demonstrating the importance of the semiconductor ink formulation viscosity and gravure cylinder cell volume to afford proper polymer film morphologies. Figure 3b shows the AFM images of optimized gravure printed vs. spin-coated ActivInk N2200 films on PET/Au substrates. Both films exhibit a fiber-like morphology, although the polymer domain sizes are ~ 10× smaller than those observed for the spin-coated films on Si-SiO_2/OTS substrates. Furthermore, the gravure-printed films exhibit a periodic

pitting (depth only ~ 2 nm for ~ 80 nm-thick film) resulting from the gravure cylinder topography. However, since both films are comparably smooth (rms roughness ~ 1-2 nm for a 20x20 μm2 area), TGBC TFTs with a ~ 1 μm-thick ActivInkTM D2200 dielectric layer can be fabricated with high fidelity (device yields > 95%). The transfer plots for equal accumulated carrier density comparing TFTs with different dielectric layer thicknesses (Figure 3c) demonstrate that also very thin dielectric films (~400 nm) can be utilized for device fabrication (entries 7 and 8, device yield > 85%). All of these TFTs exhibit remarkable performance with μe's ~ 0.2 cm^2/Vs, I_{on}:I_{off} > 10^6, and Von ~ 0~+5 V. Although it is not the scope of this report, note that TFTs based on flexo- and inkjet-printed films of ActivInk N2200 can also be fabricated (see Fig 3b for rapresentative film morphologies and and Fig. 3c for typical TFT characteristics).

Figure 3d shows the gate voltage-dependence of the saturation [μe(sat)] and linear [μe(lin)] region mobilities for two representative spin-coated and gravure-printed devices calculated using standard FET equations. In combination with the transfer plots shown in Figures 2 and 3c, these data demonstrate the high quality of both the semiconductor-insulator and semiconductor-contact interfaces. First, the rapid increase of μe(sat) to the largest value and the very small subthreshold swing clearly indicate a very low density of shallow trap states at the D2200/ ActivInk N2200 interface. The trapped charge densities at room temperature (Ntmax) for these devices, calculated from the S values, are ~ 0.5-1×10^{12} cm^{-2}, which are very low for solution-processed devices. Second, the linear and saturation mobilities are similar for both spin-coated and printed devices. In general, the higher conductivity of the channel in the linear region results in lower estimated mobilities for devices in which the contacts provide an appreciable fraction of the device resistance. This effect is present for the spin-coated devices, but the difference between μ_e(sat) and μ_e(lin) is minimal (~5%) over the range of conductivities tested. This result coupled with the lack of significant second-order curvature in the low-V_{SD} region of the output characteristics (Fig. 2a Inset), testifies to the high-quality of the contacts. The mobility variations with V_{SG} are more pronounced for the gravure-printed devices, probably due to the thicker gravure-printed vs. spin-coated semiconductor films (~ 80 vs. 40 nm, respectively). In a staggered TFT architecture (such as TGBC), overly thick semiconductor films manifest themselves in the electrical characteristics as higher contact resistances. While the overall performance of the gravure-printed devices is very good, this result suggests some room for additional improvement by reducing the printed semiconductor film thickness.

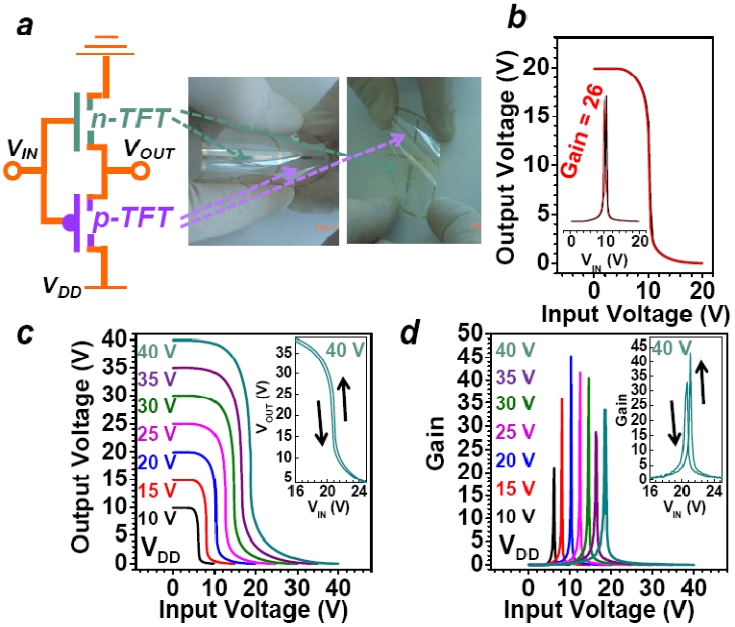


Figure 4. P3HT (p-channel)- ActivInk N2200 (n-channel) complementary inverters. a. Schematic electrical connections of the inverters and optical image of the gravure-printed device before common gate deposition. b. Static switching characteristics of an all- gravure-printed inverter (Inset: Gain on the corresponding device). c. Static switching characteristics of a spin-coated inverter. d. Gains of the corresponding spin-coated devices.

Finally, p-channel TGBC polymeric transistors were fabricated using poly(3-hexylthiophene) (P3HT) as the hole transporting semiconductor and Au/ActivInkTM D2200 as the contact/dielectric materials. These TFTs exhibit hole mobilities of ~ 0.01-0.08 cm^2/Vs, I_{on}:I_{off} = 10^3-10^4, and V_{on} = -20 ~ -5 V. Due to our n-channel polymer robustness,

excellent TFT performance with high workfunction metal contacts, and compatibility of our dielectric material with both p- and n-channel semiconductors, polymeric complementary logic with a single materials set and operating in ambient is possible for the first time. Complementary inverters having P3HT (p-channel) and ActivInk N2200 (n-channel) transistors were fabricated following two procedures, one in which both the p-/n-channel semiconductor and dielectric layers were spin-coated and the second in which all layers were gravure-printed. Figure 4a shows an optical image of the printed inverters without the common top-gate layer used as input voltage (V_{IN}). For both devices inverter response is clearly observed for switching between logic "1" (10-40 V) and logic "0" (0 V) (Figs. 4b and c). All inverters show remarkably small hysteresis reflecting the transistor threshold voltage stability. The voltage gains for the gravure-printed (Fig. 4b inset) and spin-coated (Fig. 4d) devices are very large ($dV_{OUT}/dV_{IN}(max) > 25$ and 45, respectively), implying that these devices could be used to switch subsequent stages in more complex logic circuits.

To summarize this section, top-gate bottom-contact n-channel transistors exhibiting electron mobilities > 0.1 cm2/Vs (up to ~ 0.85 cm2/Vs) in ambient with Ion:Ioff> 106 and steep turn-on have been fabricated by spin-coating as well as gravure, flexo, and inkjet printing the semiconducting layer, demonstrating great processing versatility. Furthermore, the first spin-coated and gravure-printed polymeric semiconductor complementary inverters exhibiting large gains (>25-60) and operating in ambient have been realized.

4. INKJET-PRINTED TFTS AND CIRCUITS USING ACTIVINK N1400 AND PBTTT

For this study, bottom-gate bottom-contact TFT architectures were fabricated. The p- and n-type semiconductors employed for the inkjet printing experiments are poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT)[6] and ActivInk N1400,[7] respectively. The Ta gate metal (160 nm) was thermally evaporated on a glass substrate, and it is either unpatterned or patterned by inkjet-printed masks and wet-etching.[8] To enable low-voltage operation it is necessary to increase the TFT gate dielectric capacitance. Our approach utilizes a bilayer gate dielectric consisting of a bottom high-k (Ta_2O_5) layer covered by a thin low-k UV-crosslinkable polymer (ActivInk D1400) film to minimize semiconductor density of states broadening, which is known to reduce field-effect mobility.[9,10] This inorganic-organic bilayer dielectric structure buffers the surface of the high-k component from the semiconductor active channel. The resulting bilayer dielectric capacitance is C_g= 32 nF/cm2. Source-drain contacts were fabricated by inkjet printing a silver-nanoparticle solution (Cabot).[11] After printing, the electrodes were sintered at 160°C for 5 minutes, resulting in a resistivity of 5 x 10^{-6} Ωcm and in channel widths and lengths of 180-500 and 60-120 μm, respectively. The inverter structure was completed by inkjet printing the PBTTT (trichlorobenzene, 5 mg/mL) and N1400 (dichlorobenzene, 10 mg/mL) solutions. The p-channel material was printed first and annealed for 30 minutes under nitrogen at 160°C; then the n-channel semiconductor was deposited and annealed at 120°C for 30 min. All measurements were performed in ambient conditions and in a dark box.

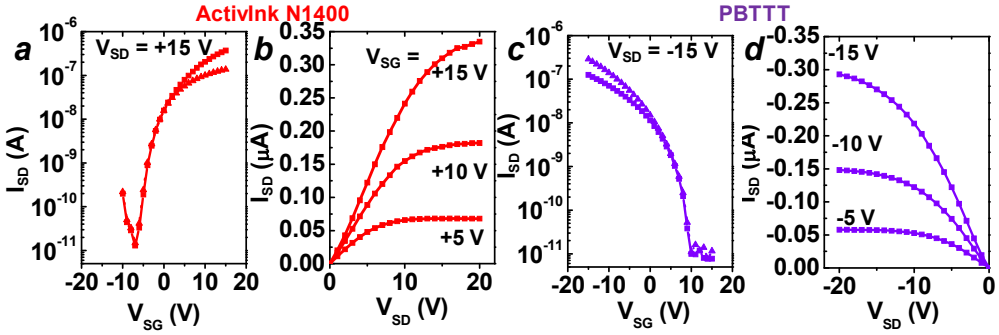


Figure 5. Transfer and output characteristics of the complementary OTFTs.

Figure 5b shows typical transfer and output plots for printed p- and n-channel OTFTs. No significant contact resistance is observed in the linear part (low V_{SD}) of the I-V output plots, indicating that the printed Ag contacts are sufficient for both hole and electron injection into the semiconductors. Typical carrier mobilities for these printed TFTs are ~0.005-

0.015 cm^2/Vs for both semiconductors with current on-to-off ratios >104. For the inverter shown in Figure 6a, both p- and n-type TFT channel width (W) and length (L) dimensions are 180 and 60 μm, respectively, yielding carrier mobilities of 0.013 cm2/Vs and 0.015 cm^2/Vs for PBTTT and N1400, respectively (± 10%). Figure 6b shows the dc output characteristics for various supply voltages V_{DD} of the corresponding inverter. The dc gain is obtained from dV_{out}/dV_{in}. Because the inverter gain is strongly dependent on the TFT transconductance at the inverting voltage V_{inv}, higher V_{DD} leads to an increase in device gain. For this inverter the largest gain value is -4.4 at V_{DD} = +20V. The inverting voltage is reached when both TFTs are operating in saturaion and is expressed by Eq. 1

$$V_{inv} = \frac{V_{DD} + V_T^p + V_T^n \sqrt{\beta^n / \beta^p}}{1 + \sqrt{\beta^n / \beta^p}}, \quad (1)$$

where V_T is the threshold voltage, $\beta = (W/L)\mu C_g$ is a design factor for adjusting the OTFT p- and n-channel currents, and the superscripts p and n denote the semiconductor type. In Fig. 6b, V_{inv} is greater than $V_{DD}/2$ due to the mobility and threshold voltage differences between the p- and n-OTFTs (Fig. 5). Asymmetry in the rise (11 μs) and fall (9 μs) times are observed in Fig. 6c, measured with V_{DD} = +10V and a square wave input from 0 to +10 V at 10 kHz. The parasitic capacitance between the gate and the source/drain electrodes leads to an overshoot of the output at the rising and falling edges. The -3dB cutoff frequency was found to be 100 kHz for 0.5Vpk-pk input sine wave and 0.02 pF load in Fig. 6d. Such performance is competitive with nMOS amplifiers using amorphous silicon TFTs.[12]

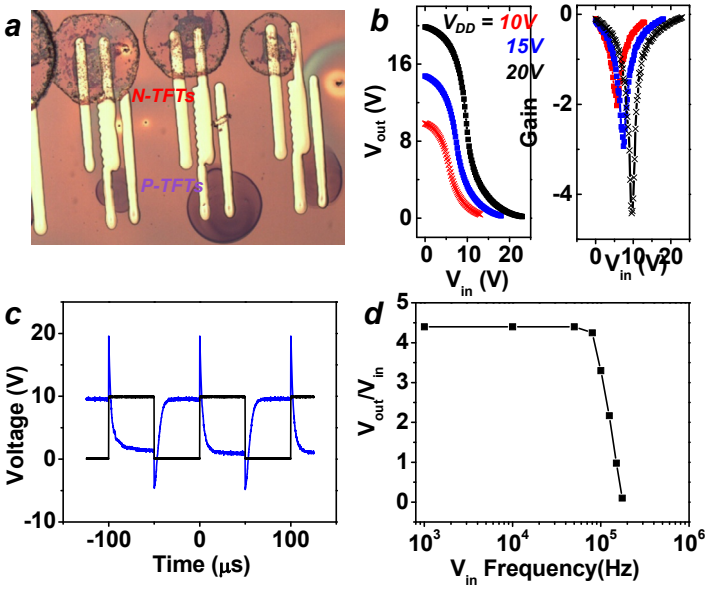


Figure 6. (a) Optical pictures of inkjet-patterned inverters. (b) Inverter output characteristics and corresponding gain at various V_{DD}. (c) Rise and fall time with V_{DD}=10V and square wave input of 0-10V at 10 kHz. (d) Inverter output/input amplitude vs input frequency. The capacitance load for (c) and (d) is 0.02 pF.

Compared to conventional silicon circuits, organic semiconductor-based TFTs usually exhibit significant VT shifts and decrease of source-drain current during operation due to charge trapping in the bandgap tail states.[13] Shifts in threshold voltages (ΔV_T) follow a stretched-exponential decay and are usually attributed to charge trapping at the semiconductor-dielectric interface. Charge trapping is accelerated by dopant impurities such as oxygen and water [13, 14] and is affected by grain boundaries,[15] dielectric surface modification,[16] and dipolar disorder from the dielectric surface.[9,10] Besides charge trapping, moisture uptake and ion movement in the polymer insulator also can also lead to ΔV_T.[17] Control over these factors has been improved, but it is still very difficult to eliminate ΔV_T. Therefore, it is important to understand and develop OTFT-based circuits such as to tolerate threshold-voltage shifts.[18] Therefore, we analyzed the relative stability of the inkjet-printed p- and n-channel TFTs and inverters for analog and digital operations.

The operation of our complementary inverters is categorized into two cases depending on the application: (1) Amplifiers in analog circuits, where input voltage V_{in} is set near V_{inv} for voltage amplification; (2) Building blocks for digital logic, in which V_{in} is set to a low or high voltage with gain less than 1. Shifts of V_{inv} are problematic in both cases, because inverter gain for input signals is unstable in the former and the noise margins[19] are worsened in the latter. From Eq. 1, a shift in the threshold voltage with time [$\Delta V_T(t)$] affects Vinv unless

$$\Delta V_{inv}(t) = \Delta V_T^p(t) + \Delta V_T^n(t)\sqrt{\beta^n/\beta^p} = 0. \quad (2)$$

In Fig. 7a, the inverter transfer characteristics shifted with time and V_{inv} was increased under constant input bias at +5.9 V and V_{DD} = +10 V. This Vinv shift indicates that the condition in Eq. 2 was not completely met and that $\Delta V_T(t)$ changes at different rates for the p- and n-channel TFTs. This behavior is evident in the relative current decay I(t)/I0 with operation time measured for the individual TFTs in Fig. 7b. The difference in bias stress rates is confirmed by analyzing the TFT transfer characteristics of Fig. 3(c), where ΔV_{Tn} = +2 V and ΔV_{Tp} = -1.5 V after 20 min of bias stress. The shift in Vinv causes the gain value at an input voltage to vary with time and, consequently, this is not acceptable for analog amplification unless complete compensation of ΔV_T is achieved.

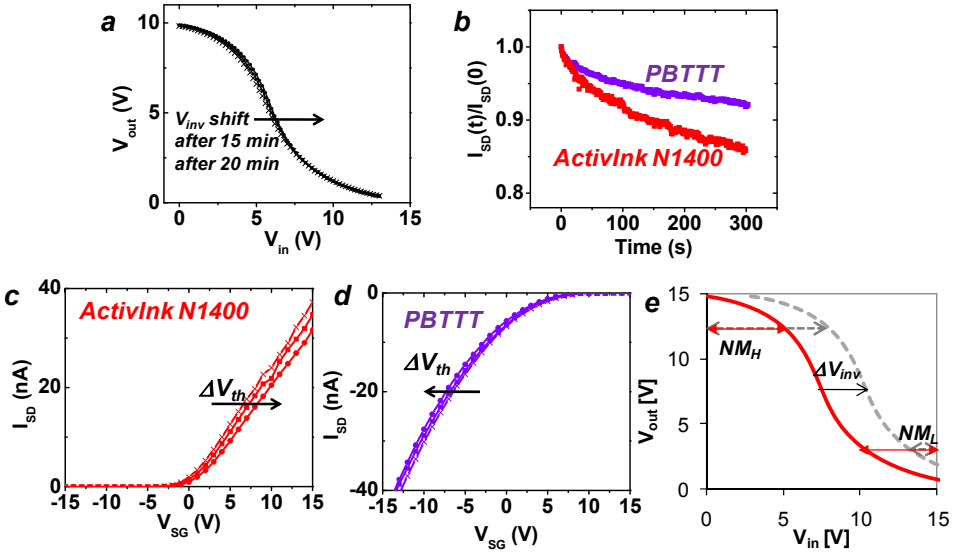


Figure 7. (a) Shift of the inverter transfer characteristics with operation time. (b) Relative current decay I(t)/I0 for the complementary semiconductors. (c,d) Threshold-voltage shifts measured after applying and input voltage of +5.9 V for 15 and 20 minutes with V_{DD}= +10 V. The source-drain voltage is at |2 V| for the transfer characteristics. (e) Transfer characteristics and noise margins (NM) for complementary inverter at V_{DD}= +15V before (red solid line) and after (dashed gray line) electrical bias stress..

However, these complementary inverters do offer considerable advantages over unipolar inverters in digital operation, by maximizing the output-voltage range and improving the noise margins. Electrical bias stress affects complementary inverters far less than those of unipolar circuits.. According to Eq. 2, the threshold-voltage shifts in our circuits partially cancel each other due to the opposite signs of ΔV_{Tp} and ΔV_{Tn} (corresponding to hole or electron traps).The change in noise margins under bias stress is estimated as follows. With the relative change in threshold voltages (V_{Tn}/V_{Tp}) approaching ~1.5 as seen in Figs. 7b and 7c and with $\sqrt{\beta^n/\beta^p} = 1.07$, the inverting voltage is increased by ΔV_{inv}=+2.9V, assuming that ΔV_{Tp} levels off to -10V and ΔV_{Tn} to +15V over time in digital pulsed operations as found in Ref. [20]. Therefore, the noise margins for the complementary inverter will be reduced by this shift in Vinvto a minimum of 1.1V at V_{DD}= +15V [see Fig. 7e]. This result still allows more stable operation in comparison with typical unipolar inverters,[21] whose noise margins were reduced below 1V at V_{DD}= +15V by a far small ΔV_{Tp} of only -0.5V.

To summarize the results of this section, fabrication of low-voltage inkjet patterned complementary organic inverters functioning in ambient was achieved for the first time. The inverter TFTs exhibit mobilities approaching 10^{-2} cm^2/Vs for

both p- and n-channel semiconductors using a bilayer dielectric and Ag contacts. The corresponding inverters operate at V_{DD} = +10V exhibit a gain of -4.4 and a -3dB cutoff at 100 kHz with 0.02 pF load. The incomplete compensation of VT shifts presents stability problems for complementary OTFT analog circuits. However, for digital operations, these inverters exhibit an estimated noise margin ≥1.1 V at V_{DD} = +15V. Therefore, our results demonstrate the greater potential of a complementary inverter technology over unipolar devices.

5. CONCLUSIONS

In summary, we demonstrated successful integration of two n-channel semiconductors with good p-channel materials for printing CMOS fabrication.

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