

## **EUV Progress Toward HVM Readiness**

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### **ABSTRACT**

This past year has witnessed a sharp increase in EUV lithography progress spanning production tools, source and infrastructure to better position the technology for HVM readiness. While the exposure source remains the largest contributor to downtime and availability, significant strides in demonstrated source power have bolstered confidence in the viability of EUVL for insertion into HVM production. The ongoing development of an EUV pellicle solution alleviates industry concern about one significant source of line-yield risk. In addition to continued expected improvements in EUV source power and availability, the ability to deliver predictable yield remains an ultimate gate to HVM insertion. Ensuring predictable yield requires significant emphasis on reticles. This includes continued pellicle development to enable the readiness and supply of a robust pellicle solution in advance of 250W source power, as well as improvements in mask blank defectivity and techniques to detect and mitigate reticle blank and pattern defects.

### **1. INTRODUCTION**

The challenges of EUV implementation for High Volume Manufacturing (HVM) remain essentially unchanged from one year ago. Resist materials must meet the resolution requirements with acceptable Line Edge Roughness (LER) at reasonable exposure doses while at the same time meet outgassing requirements. The exposure source must provide adequate power and availability, with the scanner hardware remaining on track in terms of availability. Reticles provide a significant risk to EUV readiness due to inadequate inspection capability combined with the significant likelihood of defects. Defects are a risk during reticle manufacturing (both mask blank and mask manufacturing) as well as fall-on particle defect adds that are introduced during normal production use. All of the elements supporting EUV technology must come together simultaneously in order for EUV to be viable for HVM. Over the past year significant progress has been made in many of these areas. Some of the historic technical issues that have been problematic in the past are improving at an impressive rate, and the pieces are coming together.

### **2. TOOLING**

#### **2.1 EUV Source Power**

When it comes to source power, progress continues toward the 250W milestone that is needed to support HVM. Recently ASML has demonstrated improvements in power scaling achieving the 200W mark while keeping the exposure dose within specification<sup>1</sup>. Figure 1 illustrates the historical source power scaling roadmap, depicting each 'reset' of the roadmap since 2010. In the past, source power has lagged well behind this roadmap, but the significant 2X improvement in source power over the past year lends credibility to the 250W roadmap needed to support HVM.

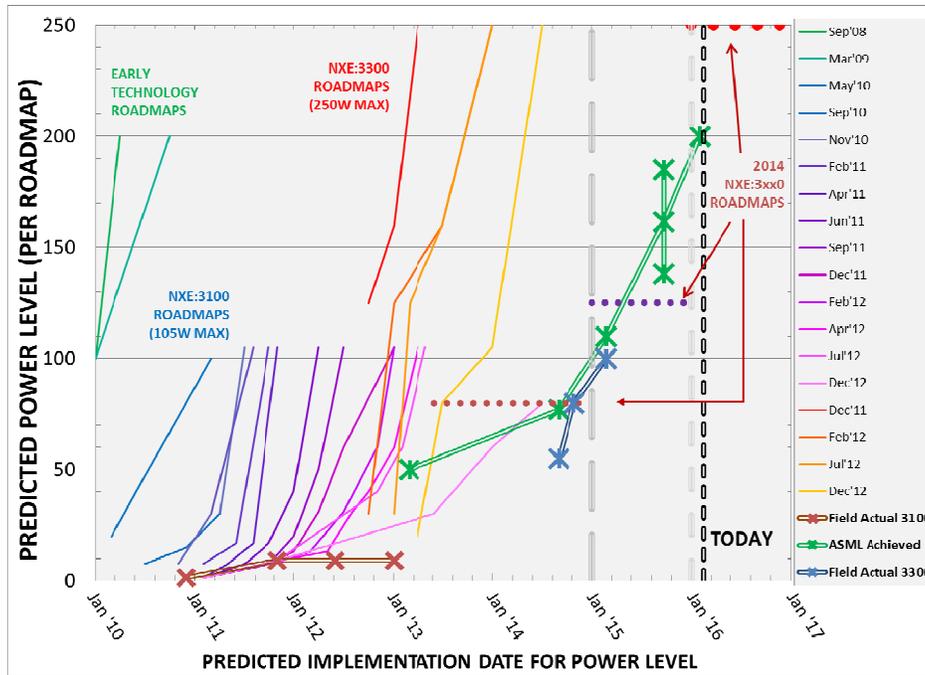


Figure 1. EUV Source power scaling roadmap

## 2.2 Droplet Generator

Over the course of the last year, droplet generator (DG) lifetime has varied greatly. Figure 2 shows the actual DG run-time relative to the expected run-time, where each data point represents the moving average of 13 DGs. In mid-2015 the DG lifetime was less than half the expected run-time; significant progress was made over the course of six months such that DG lifetime now averages about 80% of the expected value. Overall, DG performance has improved more than 3X with the majority of DG swaps that occur before the expected end-of-life being forced as a result of other machine issues.

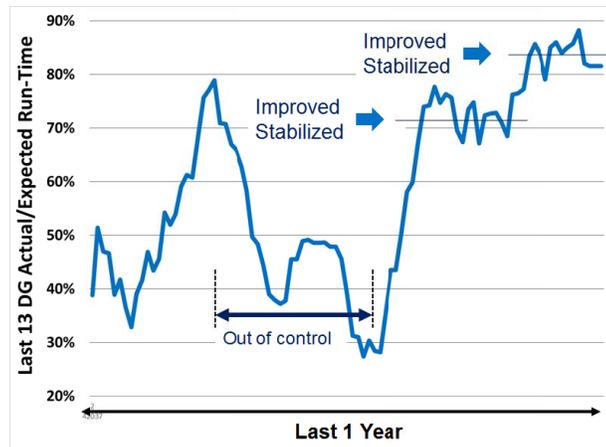


Figure 2. Droplet generator actual vs. expected run-time

## 2.3 Collector

Another significant factor affecting source availability is the collector. Figure 3 depicts wafer throughput (TPT) as a function of pulses on the collector relative to the TPT of a new collector. Collector reflectivity

degrades with usage, decreasing TPT as the collector accumulates pulses. The collector reflectivity and TPT losses are linear and, as such, are predictable. On top of this predictable trend are continuous improvements in the collector lifetime, which lend credibility to the projected collector lifetime that fabs are building into planning models and operating costs.

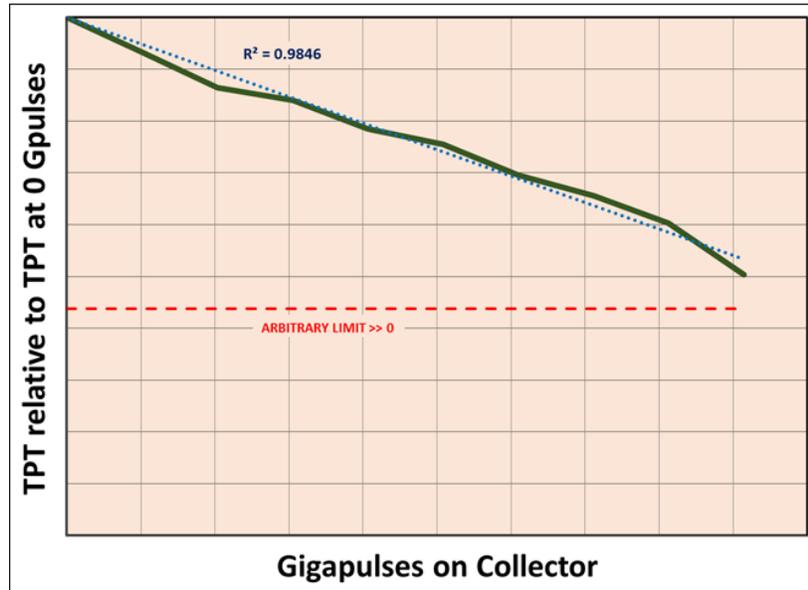


Figure 3. Wafer throughput vs. pulses on the collector

## 2.4 System performance: 14nm EUV pilot line

Lifetime and reflectivity are the appropriate metrics to use in considering the source. The most accurate way to measure availability and productivity metrics, however, is to exercise the tool in production mode. An extended demonstration of the NXE:3300 in the 80W configuration is in process in which 21 hours of the day are dedicated to printing wafers (comprised of a mix of test chip and bare silicon). Availability is metered 24hrs/day, and only wafers satisfying the exposure dose specification are counted. Combined scanner/source availability is a key metric of the extended NXE:3300 demo, and the combined 4-week availability has been running relatively steady around 70% which is on par with the target for the system in the current configuration. Overall availability and productivity is sufficient to support ongoing development work. This work supports a 14nm pilot line utilizing complementary patterning with 193 immersion, with EUV being leveraged for via and cut layers. The demo runs wafers in production mode and monitors patterning performance including CDs and overlay as well as electrical testing and end-of-line (EOL) yield results. Figure 4 provides a comparison of x- and y- overlay error between EUV and 193 immersion processing of the 14nm pilot line. Here each data point represents one wafer and each cluster of data points represents one lot of wafers, with the EUV data in green and 193 immersion in red. It's clear from this data that there is not an overlay penalty for EUV-193i versus 193i-193i MMO.

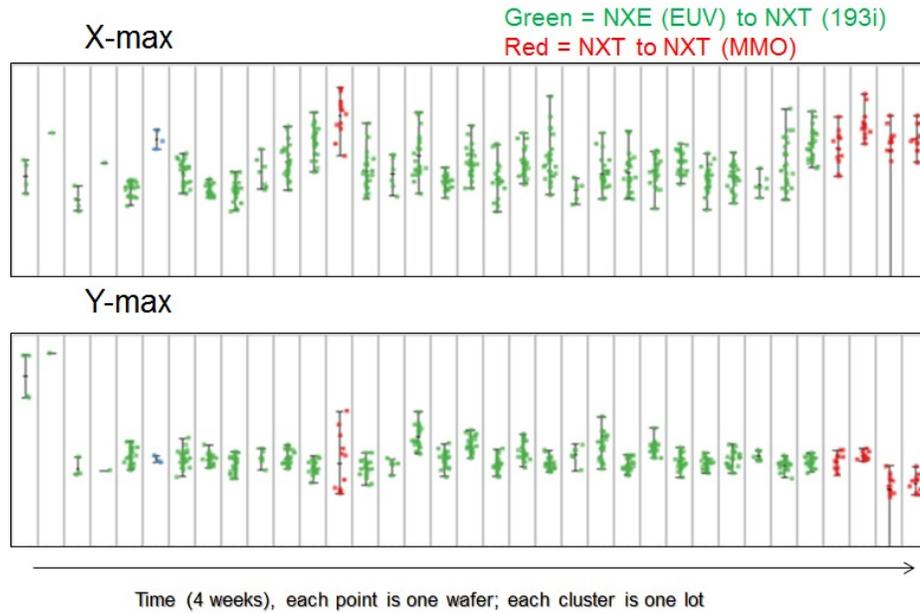


Figure 4. 14nm EUV pilot line x- and y- maximum overlay performance comparing EUV to 193nm immersion

Via Critical Dimensions (CDs) were measured as part of the 14nm pilot line. Figure 5 shows a seven-month trend of two different via CD metrics, plotting the difference between the actual measurement and the intended target size. Potentially disruptive events in the form of two resist batch changes and one collector replacement occurred over the course of the seven months shown in the graph. CDs remained relatively stable while the exposure dose was not adjusted in response to either the batch changes or collector change.

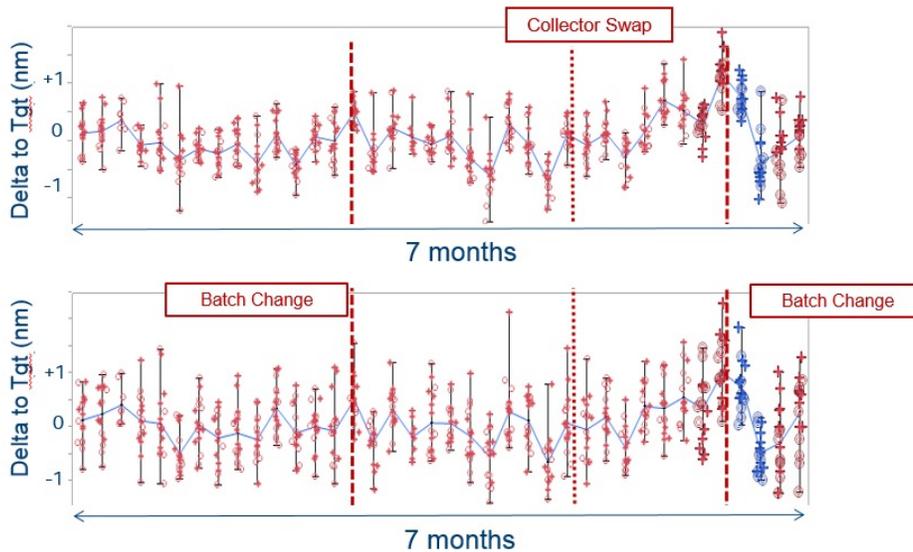


Figure 5. 14nm EUV pilot line CD performance without exposure dose change

In addition to measuring litho patterning performance with the pilot line, electrical performance as well as EOL yield were measured compared to a 193nm immersion baseline. Figure 6 illustrates six months of via (single and chain) resistance for five different via sizes. The data from the 193 immersion Process of Record (POR) is depicted by the red data points in the far left in each of the via size bins. All of the remaining data within each bin are EUV lots. It's clear from this data that the 14nm EUV pilot line demonstrates stable EUV electrical performance over this period, and it is equal to or better than 193i. On the right is a graph showing an End Of Line (EOL) yield comparison between EUV and 193i splits where each data point represents one wafer. Here we see that EUV yield is roughly matched to 193 POR.

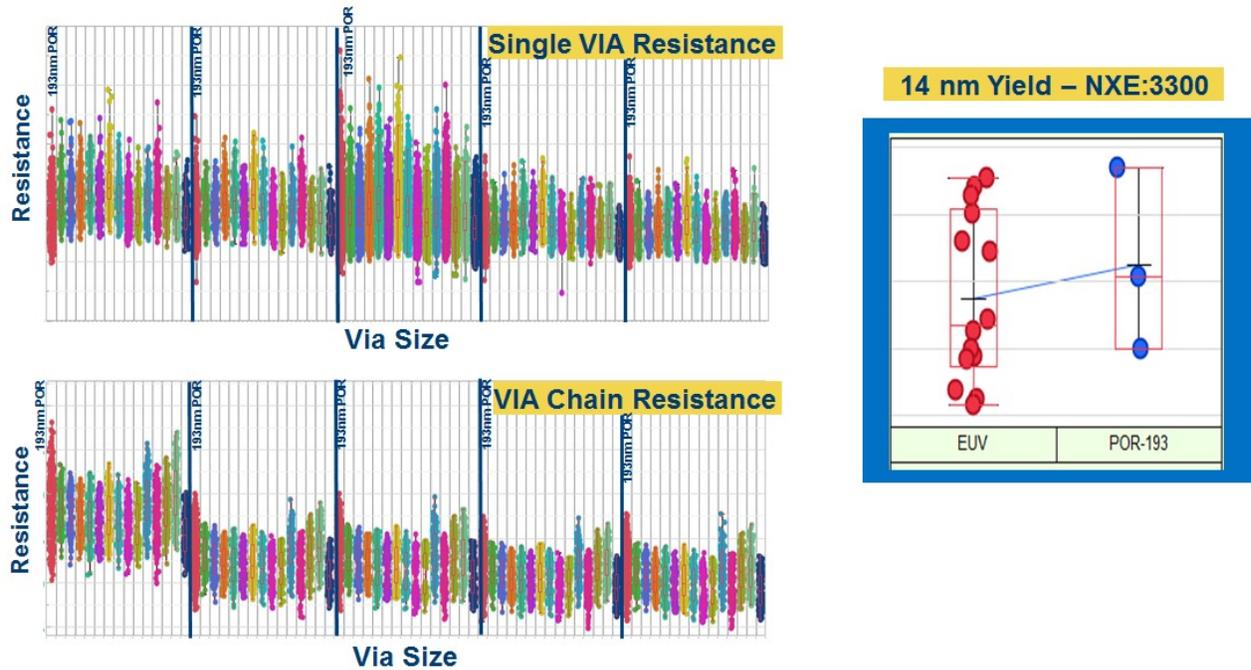


Figure 6. 14nm EUV pilot line via chain resistance and end-of-line yield comparing EUV to 193nm immersion

As demonstrated by the data above, solid progress has been made over the past year in key aspects of EUVL tool performance including source power, droplet generator and collector as well as the system availability. In addition, 14nm EUV pilot line data shows equivalent or better performance compared to a 193nm immersion baseline for patterning performance, electrical testing and EOL yield results.

### 3. RETICLES

Similar to the 14nm EUV wafer process pilot line, an in-house pilot line is also running for EUV masks, exercising the full mask process flow.

#### 3.1 Reticle defectivity

Reticle defects remain the most significant area of concentration and include defects generated during the blank- and mask-making process in addition to those reticle adder defects induced as part of normal fab

and scanner operation. Reticle blank manufacturers continue to reduce the number and size of Multi-Layer (ML) defects. Multiple suppliers are capable of producing blanks having single-digit level defects, and large defects are mostly eliminated on quality blanks today. The availability of Actinic Blank Inspection (ABI) has enabled this continual defect reduction trend, which needs to continue in order to improve mask quality, yield and cost.

### 3.2 Reticle defect mitigation and repair

Mask blanks with defect counts in the single-digit level can benefit from defect mitigation by pattern shifting in which the design pattern is translated in x- and y- on the mask blank in such a way that defects contained within the mask blank are covered by absorber material. This technique is accomplished more easily on dark field masks which have larger areas covered by absorber material. The pattern shift mitigation flow includes pairing a specific layer pattern with a mask blank that contain fiducials. The mask pairing and pattern shift computations require fast data automation as well as alignment accuracy during the pattern write. Ultimately the success of the pattern shift must be verified, and to do this within the confines of the mask shop requires the use of AIMS. Figure 7 demonstrates a 7nm node dark field defect-free mask in which defect mitigation by pattern shifting rendered all defects unprintable<sup>2</sup>. Defect mitigation by pattern shifting is a complicated process, so it remains critical to continue driving down defect levels in mask blanks.

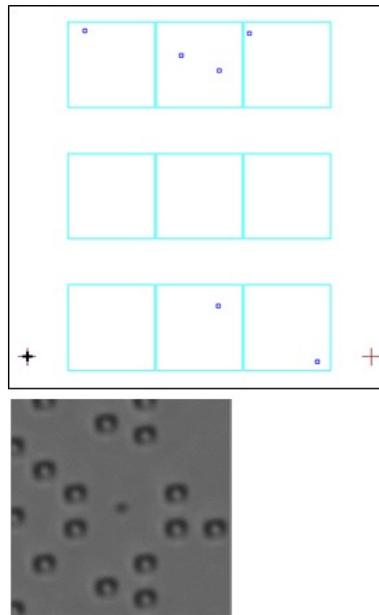


Figure 7. Defect mitigation by pattern shifting for DF (7nm node) mask, with the defect in the center of the image covered by absorber material

Defect mitigation by pattern shifting is one aspect of the EUV mask pilot line; another area of emphasis is defect repair, in the form of both patching and cutting repair. Patching repair entails adding absorber material to compensate for a defective area, and cutting repair involves removing sections of unintentional absorber material. Both patching and cutting repair examples are illustrated in Figure 8 along with the resulting aerial image intensity and SHARP microscope images resulting from the

patching repair. Using a combination of pattern shifting along with mask repair, Intel Mask Operations has successfully produced multiple EUV masks with zero printable defects.

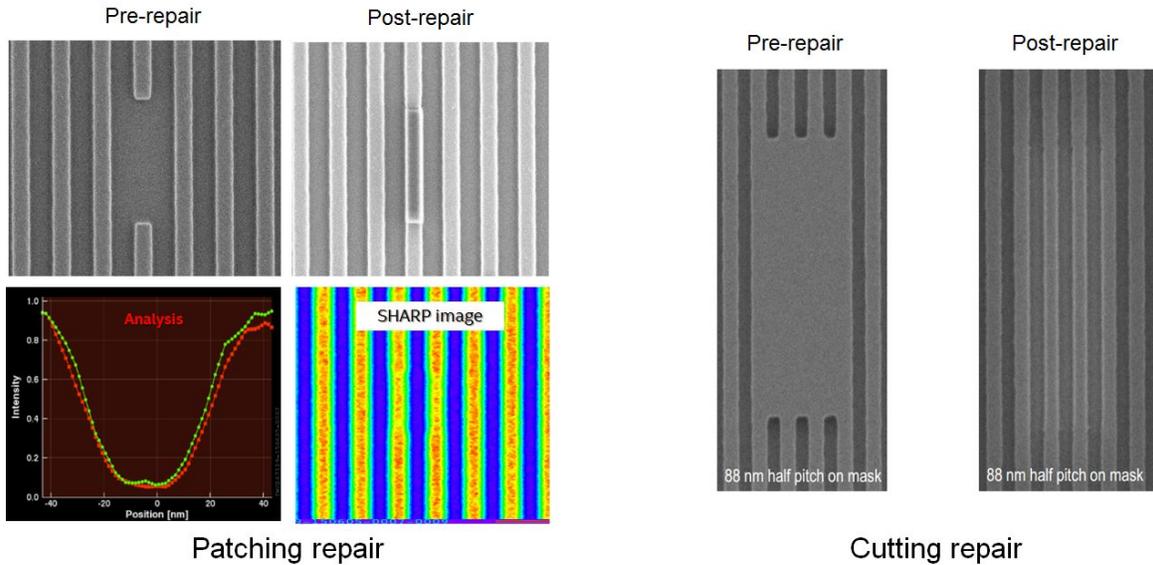


Figure 8. Examples of cutting repair (with resulting aerial image intensity and SHARP microscope image) and cutting repair

### 3.3 EUV Pellicles

Defect mitigation and e-beam mask repair have the ability to enable defect-free masks. However, a mask that is initially defect-free becomes a yield risk as a result of fall-on particles in the scanner environment. Front-side reticle defect levels continue to reduce with system improvements over time and with the introduction of each new scanner platform<sup>3</sup>. While the reticle defectivity trend is encouraging, in the absence of a pellicle, there must be zero fall-on reticle defects to ensure that there is no impact to product yield. Figure 9 shows the number of added defects per reticle stage load from two different NXE:3300 scanners over the past six months, measured using optical scan of printed wafers.

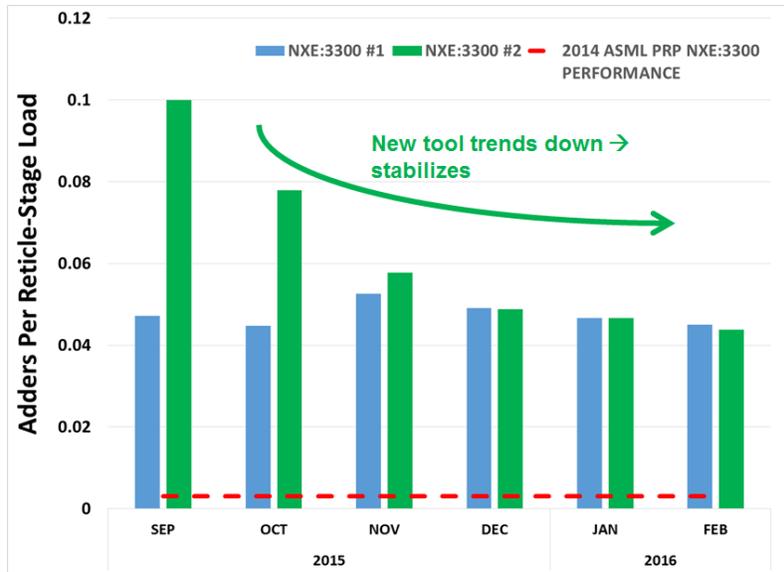


Figure 9. Number of reticle defects added per reticle-stage-load as measured using optical scan of printed wafers.

Every printable reticle adder defect represents a potential yield-limiting defect, and wafer fabs today mitigate this risk for DUV masks with the use of a pellicle. Over the course of the 14nm EUV pilot line, measurable EOL yield degradation has been observed due reticle adder defects; hence, the emphasis on commercial pellicles must continue. Since ASML embarked on a full pellicle solution<sup>4</sup>, there has been significant progress in pellicle development. Pellicle mounting and support tooling is being tested and made available to customers, pellicle defect inspection is in development, and pellicle transmission measurement capability is available. In addition, a full-field 40W pellicle membrane has been used to expose >200 wafers, being handled by customers and shipped from ASML to Intel multiple times, with the pellicle film remaining intact. The pelliclized reticle exposures provide insight into the efficacy of the pellicle frame design, which has mitigated reticle adder defects in tests completed to date. Existing particles on the pellicle also do not appear to migrate across the reticle surface, and studies are underway to quantify imaging impacts. While the pelliclized reticle test results provide compelling benefits, a commercially viable high power (250W) pellicle membrane material has not yet been developed. It is the availability of quality pellicle membranes which presents the highest risk to timely EUV pellicle implementation. With pelliclized reticles, in-fab inspection is needed to ensure predictable yield. The current lack of commercial Actinic Patterned Mask Inspection (APMI) is not a show-stopper, but without it, yield and cost may be an issue.

#### 4. CONCLUSIONS

EUVL technology is solidly on a path to HVM insertion which is highly desirable for the 7nm logic node, but the final decision will be based on technology readiness and cost effectiveness. There has been significant progress in photoresist development as materials suppliers continue to make inroads toward reasonable exposure doses in patterning tight feature sizes. Suppliers need to consider novel materials while at the same time not be overly constrained by outgassing tests when determining experimental

formulations. Significant progress in source power toward the 250W projected roadmap along with concurrent improvement in source lifetime metrics provide credibility in achieving the performance needed to support HVM. 14nm EUV pilot line wafer data demonstrates matched overlay, CD, electrical test and EOL performance between EUV and 193nm immersion baseline. Yield risk remains as a result of reticles, and while defect mitigation and repair techniques have been successfully demonstrated, they are complex, costly and time-consuming. Protecting a defect-free reticle in the scanner and fab environment requires the use of a pellicle; this development needs to be accelerated. Technology development activity requires rapid information turns: tools must be up to run development wafers without delay. As such, system availability is the critical, gating concern today.

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