Etch aware computational patterning in the era of atomic precision processing

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ABSTRACT

Etch processes have always involved inherent process trade-offs related to fundamental plasma parameters to achieve planar patterning metrics related to damage, aspect ratio dependences and profile. Today, we are in a new era of "area selective etch." Advanced patterning (SAXP, $(LELE)_n$), logic, memory and interconnect applications beyond 3 nm involve, in one way or another, topographies that require etch "control" at every surface. Achieving profile specifications will require the ability to conjure isotropy control at will. Vehicles to achieving this include novel precursors and hybrid processes involving combinations of deposition and plasma etch as we know it. Ultimately, to differentiate surfaces comprising silicon, silicon oxides and nitrides, and organics require active modification at the first surface reactive monolayer to be able to differentiate them in each process step with respect to any surface normal on the wafer plane. This presentation will start with a review of today's state-of-the-art means for atomic precision processing of surfaces. A simulation science perspective to process integration modeling introduces methods for surface chemistry control that lend themselves to achieving area selective etch. In the end, surface chemistry control is not a cure-all. Finally, a combination of plasma diagnostics and simulation will be needed to assist plasma process controls for scaling at 3 nm and beyond.

Keywords: plasma etch, simulation, patterning, first-principles models

1. INTRODUCTION

Etch-aware computational patterning conjures images of lithography models for photomask prediction "nudged" to accommodate non-optical unit processes. With emerging complex 3D devices brought to realization by a myriad of unit processes, primarily dry etching, understanding the impact of the thread of lithography and other unit processes on final device integrity is extremely important. To be impactful for technology development, computational patterning must comprehend device integration and adapt the new processes and chemistries that will be used at 3 nm. Therefore, it is timely to reflect on exactly what etch-aware computational patterning, and for that matter, etch computation means.

1.1 Optical Proximity Correction and Computational Lithography

Resolution enhancement is a good beginning point for a discussion of etch corrections. Resolution enhancement techniques enable photomasks to print sub-resolution patterns through the development of photoresist materials spun on substrates that act as masks for etching/cleaning and final structure construction. Becoming necessary in the 1990s when critical dimensions decreased to well below available optical wavelengths, these techniques included the placement of scattering bars, serifs or assist features, in general, on patterns, the use of phase shift masks (PSM) and, later on, multiple patterning (double, quadrupole, either self-aligned or litho-etch sequences).

At its most elemental, there are two tasks for patterning: layout of the contours of the mask structures on the substrate and realization of desired profiles. Both tasks involve computation; hence, computational lithography. Independent of other biases, etch through a mask pattern would replicate the desired features. With respect to layout, if uncorrected, the blurring/distortion of projected images developed on photoresist (As Developed Image or ADI) due to diffraction through closely spaced structures, would lead to deviation of the final etched and cleaned structure (As Cleaned Image or ACI) away from the target structure. Correction to the photomask layouts (*e.g.*, the placement of serifs, movement of edges, and addition of structures) due to the proximity of structures at sub-resolution dimensions is optical proximity correction (OPC). OPC involves computation based on "light physics" models for the movement of "edges". Photoresist profile is important as it affects the etch steps that follow. How photoresists are exposed and developed is determined either experimentally or through more computational models. As Developed Images are also well represented by "light

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physics" models. Erdman *et al.*, is representative of classic predictions of how developed structure profiles varied with different exposure conditions. [1] The two computational efforts, photomask definition and profile prediction, are related in that an edge of a final 2D structure derives from a cut plane through a feature profile.

Considering the lithography unit process on its own, design of photomask to ensure replication of targeted structures post development is a resource heavy complex numerical task. Full profile simulations are impractical and simulations for "fracture" are carried out with a minimum of information about the device layout (edge location and view factor information). Sezenger *et al*. illustrates one approach. [2] Recent work by Ma *et al*. [3] indicate the sophistication of today's OPC technology. [4] All in all, consideration of etch bias should not add significantly to the complexity or computational load.

1.2 Introducing Etch Process Bias

Final structure fabrication involves multiple etching steps through developed masks and, finally, cleaning steps. Each influences ACI profiles. One problem for OPC approaches is that etch, cleaning and deposition processes are not well represented by the light physics models on which OPC models are based. A second problem is that predicting the edge movements (biases) of physical structures due to a train of etch steps following a development step may not even be a well-posed problem. Formation of sensitive structures involved at the very least a main and often multiple "over" etches and so-called soft landings. These individual processes could introduce aberrations in profiles not well represented by a single "edge". Early on, the role of etch bias, independent of lithography bias (etch variations from the developed structures), was recognized and reasonably well understood. [5] Etch variations correlated well enough with lithography variations or were a small enough source of error that through-pitch test vehicles could be used to correct errors and adjust edge placement models ultimately used to create masks. Process margins were also such that process engineers could manage aberrations that showed up in the etch unit processes. It could be fairly stated that features could be defined by lithography but the topographic and material characteristics that defined electrical performance were defined primarily by etch unit processes (*i.e.,* process engineers themselves).

1.3 Etch Driven Scaling

Soon replication of critical dimensions was impossible even with 193 nm, immersion, PSM and OPC technology. EUV was not introduced in time for the dimensional shrinkage accompanying new technologies. Plasma etch processes solved this problem. Trimming of mask structures using plasmas, the thinning of lines without complete erosion of the line, allowed the formation of smaller critical dimension structures. This alone did not solve the need to print features at increased density. Double patterning involving multiple etch steps (*e.g.*, SAXP, LELE), deposition and sometimes multiple exposures solved this problem. Now, unit processes other than lithography drive precision dimensional control and so dominate sources of variation. Even if EUV were able to be fully engaged today, etch based process integrations comprising halving or quartering developed mask geometries are needed for scaling. The spatially subtractive nature of plasma based etch relies on ion angle control to facilitate today's nanoscale devices. This is desirable for aggressive pitch scaling provided ion energy and angle control scales as well. Additive methods based on deposition generally lack ion driven control. As such, for the near future, understanding how technology will scale to 3 nm and beyond requires awareness of how plasma etch processes manipulate surfaces at the atomic scale.

The theory of this discussion is that etch processes rather than lithographic steps will control patterning scaling. Therefore, etch-aware "computational patterning" is a critical need for advanced device manufacturing. However, what exactly constitutes etch or process aware computational patterning merits consideration. How to deliver atomic scale precision on topographic devices with new materials using computation is an open question. What role do physics based models play, what degree of concurrence with experiment is needed and how much calibration is needed are all questions at the fore. In particular, with new materials and new digital processes (atomic layer etch, atomic layer deposition and selective area processing) being implemented, the key question is what role first principles models can play. What exactly constitutes etch aware computational patterning and what will its impact be in process and device development is the focus of this note.

2. PROCESS AWARE COMPUTATIONAL PATTERNING: A LOOK BACK

There are two aspects to dealing with etch processes in computational patterning: 1) choosing whether to segregate the individual process steps (lithography and etch) while establishing the photomask geometry and 2) describing the unique three-dimensional transport within topographic structures that leads to process (etch) bias and accounting for it in bias

and profile estimation. Adjustments to edge placements in phase shift masks (PSM) to account for all process variations (optical, CMP, etch) evolved in rule or model based forms. "Rules" based on experimental results from test structures capturing the ADI to ACI transition were an early approach allowing etch and lithography models to remain one. Models were risky as topographic corrections involved solid angle dependent species flux shadowing effects that could not be well captured by line and space experiments or by light physics models and as will be discussed, multiple etch steps could confound many biases into one. As long as etch biases were not dominant and variations could be addressed by process, these approaches worked well.

2.1 Kernels and Model Based Approaches Accounting for Etch

Deriving functions that would describe etch biases for model based corrections required analysis of two-dimensional (on the wafer plane) etches of test structures of differing density so species transport sensitive to view factor effects could be taken into account. Following Zavyalova *et al.,* a lithography model *L* intakes a mask pattern *M* and outputs a resist pattern *X*: *L(M)=X*. Then, an etch model *E* takes a resist pattern and *X* and outputs an etched wafer pattern *D*: *E(X)=D*. [6] The etch bias (difference between the developed resist and etched edge positions) is a function of the visible open area (to be etched), degree to which the feature view is blocked and the density of material to be etched (loading).

Description of the etch process, *E(X)=D*, in a manner tractable for OPC models has always been problematic. If the developed resist contour geometry is sufficient to describe the final etched pattern then as Weisbuch *et al.* point out, geometric functions "kernels" ought to be enough. [7] Sato *et al.* demonstrated this exercise in their early work. [8] Shim and Shin describe the etch bias (*EB*) as,

$$EB = (X - D) = A_o + \sum_{n=1,\ldots} B_n Den^n + \sum_{n=1,\ldots} C_n Blo^n + \sum_{n=1,\ldots} D_n Vis^n \quad (1)$$

where *A*'s, *B*'s, *C*'s and *D*'s are fitted parameters and *Den, Blo* and *Vis* are density, blocked and visible "kernels".[9] Fig. 1, adapted from Ref. 9 is a schematic visualization of factors embedded in kernels affecting edge bias, the lateral movement of the segment of interest. Den is representative of the degree to which species such as radicals are consumed or loaded down by the etchable areas $a_{1,2,3}$. *Blo* and *Vis* are indicative of the solid angle view factors due to blocking structures and etchable (visible area) region in front of the edge segment.

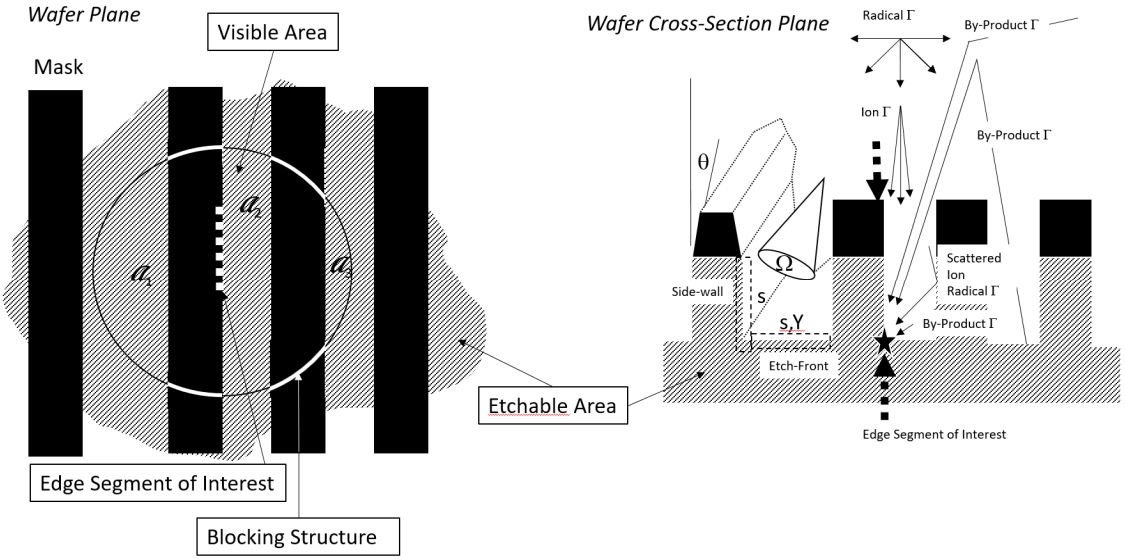

Figure 1. Wafer pane and cross-section plane illustrating factors that affect edge etch bias (lateral movement of an etchable edge segment of interest relative to the developed mask edge). The cartoon kernel is represented by a circle around the edge. Within it are the density, blocking and visible kernels. A's represent etchable area regions, s represents sticking coefficient and Y represents etch yield. The cross-section view shows how species (ions, etch precursors (radicals) and etch by-products) reach the side-wall and etch front medicated by solid angle view factors (Ω), etch yields (Y) and sticking coefficients (s).

For a single etch step depicted in Fig. 1, the kernels are representative of the impact of view factors and etchable "open" area on the flux and energy that reach the feature edge and etch front, direct and indirect by-product deposition. An alternative to representing etch biases by density, visible and blocking kernels would then be to use physics-based expressions that account for the same phenomena. With reference to Fig. 2, the etch bias at δ below the mask bottom can be described by Eq. 2 assuming the vertical etch profile remains horizontal. The etch bias is a function of the ion flux (Γ_{ion}) at angle (θ) from the wafer plane normal, etch yield Y as a function of energy and the angle of incidence (α) with respect to the surface normal (n), the material density (ρ) and the flux (Γ_{bp}) and sticking coefficient (s) of etch byproducts or deposition precursors.

$$EB(@\delta) = (X - D) = \int_{\Omega(\delta),t=t(\delta)}^{t=t\_stop} dtd\Phi d\theta \sin(\theta) d\varepsilon \frac{\Gamma_{ion}(\delta,\theta,\Phi\varepsilon)\sin(\theta)}{\rho}(\varepsilon,\theta)Y_{\varepsilon}(\varepsilon)Y_{\alpha}(\alpha) - \int_{t=t(\delta)}^{t=t\_stop} dt \frac{s}{\rho}\Gamma_{bp} \quad (2)$$

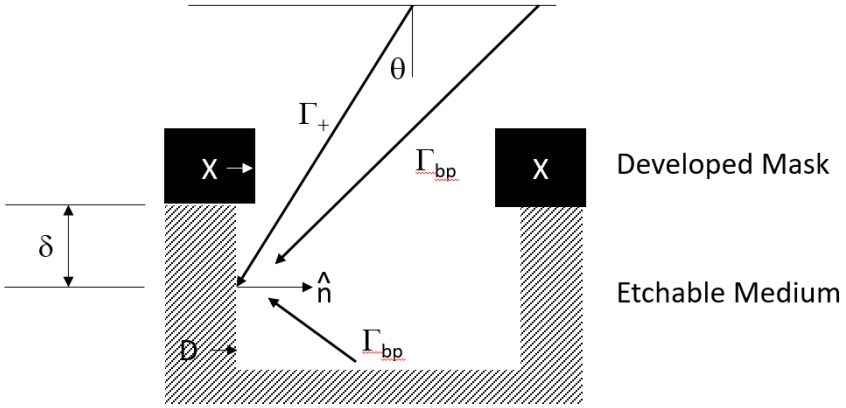

Figure 2. Schematic representation of how local ion flux and etch by-products (or deposition precursors) interact with a sidewall edge (D) beneath developed photoresist with edge X.

Percin *et al.* provided an example of etch physics embedded in some manner in edge placement models. [10] Models for the etch process could be derived from experiments and based in simple phenomenological etch models as in Senziger *et al*. [11] Phenomenological etch models had been extremely successful in explaining important through pitch etch (line and space) behavior such as "RIE" Lag.[12] In this sense, the efficacy of incorporating phenomenological etch models as described by Senziger *et al.* was not surprising.[11] This approach, however, relies on the etch step being a single step or, if multi-step, that only one etch step dominated the edge variations or CD bias of the many.

In practice, the etch processes need to be finessed to correct for profile deviations from patterning model predictions. Computational patterning comprehended profile for the first time with the work of Cooperburg *et al.*[13] In this work, measured profiles tuned a phenomenological feature scale model. In principle, the model aids navigation within the tuned parameter space with the aim of adjusting a process to meet feature geometry requirements. Feature scale simulations with sufficient fidelity and adjustable parameters to capture plasma etch through pitch biases gradually evolved [14] that were good analogues of the work of Erdmann *et al.* [1] for a single etch process step. The explicit consideration of the impact of ADI profile on subsequent etch bias in an OPC model was demonstrated by Wu *et al*. with some good success. [15] Considering the ion flux at δ in Eq. 2 and Fig. 2, could result from the scattering of ions by the mask, a correction factor accounting for the photoresist sidewall angle (SWA) was included. Equation 3 represents their correction based on a compact model for ion scattering,

$$EB = c_o + \frac{c_1}{\tan(SWA)} + f\left(p_{refelction}(SWA)\right). \quad (3)$$

Concurrent use of physics-based etch feature scale models and process experiments for computational patterning unfortunately was not widely adopted. One reason for this was that rapidly increasing complexity of plasma processes and the multi-step nature of processes for the fabrication of single features.

2.2 Integration Modeling and Rule Generation

Multiple critical etch steps to form single features and lithography aids like trim and double patterning steps managed to continue Moore's Law scaling; it would otherwise have stopped when EUV was not ready to be adopted. Integrated plasma equipment – feature scale models evolved to be able to replicate trim [16] and multiple etch steps.[17] Etch by-product redeposition, deposition from plasma generated species and passivation and lack of passivation from sequences of etch steps renders no linear relationship between the incoming developed structure and final cleaned structure.[18] Fortunately, the computational heft available to simulation scientists increased allowing feature scale simulations of multiple processes over arrays of features important to being able to capture important etch biases such as line end pullback.

Figure 3 includes an example of an etch partition between development and final clean, taken from Stout *et al.,* that illustrates the complex relationships between features from each etch step.[19]

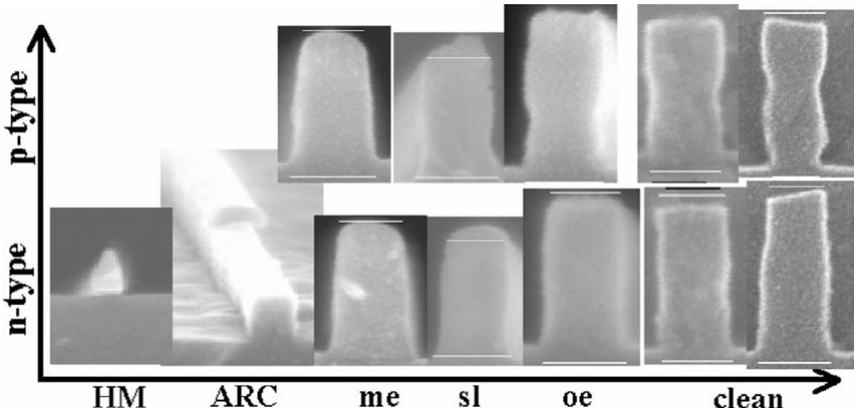

Figure 3. Experimental cross sections of parallel lines at certain stages in the gate etch process (HM hard mask, ARC antireflective coating, main etch, soft landing, over etch and clean) for p- and n-type polysilicon. (*Reprinted with permission from J. Vac. Sci. Technol., B (24), 1810 (2006) [Copyright 2006], American Vacuum Society.)*

Stout *et al.* demonstrated the ADI to ACI profile evolution of an SRAM bit cell in the same study.[13] Importantly, this study included a prediction of the bit cell photoresist profile from a contour extracted from a model of the exposure through the photomask. A FinFET integration was also demonstrated. Figure 4 includes examples of SRAM bit cell and FinFET integration simulations.

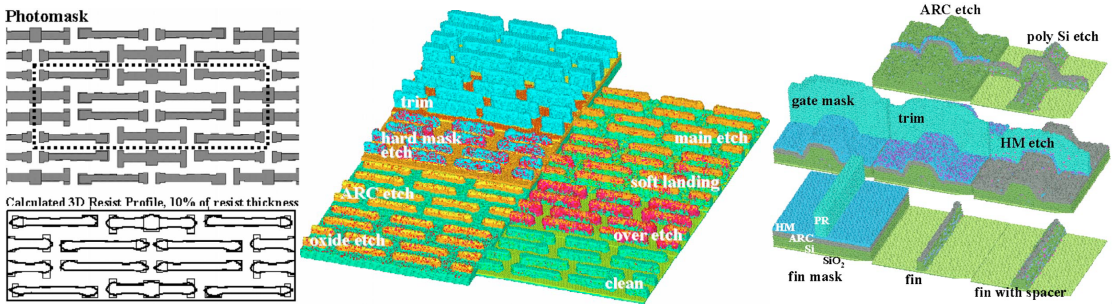

Figure 4. Photomask layout and predicted photoresist contours for an SRAM bit cell; the evolution of each of the etch steps needed to fabricate the bit cell and a FiNFET integration predicted by integrated equipment-feature scale simulations (*Reprinted with permission from J. Vac. Sci. Technol., B (24), 1810 (2004) [Copyright 2004], American Vacuum Society.)*

The temptation at the time was to believe that this formalism (coupled photomask, exposure, feature scale topography evolution and plasma equipment models) could be used to adjust photomask edged to correct for etch biases. At the

time, the integration of photoresist exposure and plasma etches in a cellular feature scale simulation was a herculean computational task involving tight coupling of the model development to partition experiments. Each plasma etch step required its own set of inputs from plasma equipment simulations (inductively coupled plasmas) each with distinct plasma chemistries. Executing these kind of simulation suites [19] in-line with a simulation tasked with moving photomask edges [5,6] was clearly not practical even with some advances incorporating compact models.[15]

A more modest approach was to evaluate through-pitch structures and create rules for edge placement based on insights from simulation results. A demonstration of the impact of such a rule on a through-pitch test structure is shown in Fig. 5. The fact was that, in the end, the effort required for this exercise was prohibitive. With no first principles models for plasma species surface interactions and sparsely populated plasma chemistry databases, extending the methodology from one technology node to the next meant going through extensive equipment and feature scale model redevelopment and calibration with materials. Experiments were a faster means of dealing with node-to-node technology changes and accounting for etch biases in mask layout or in subsequent process development for high volume manufacturing.

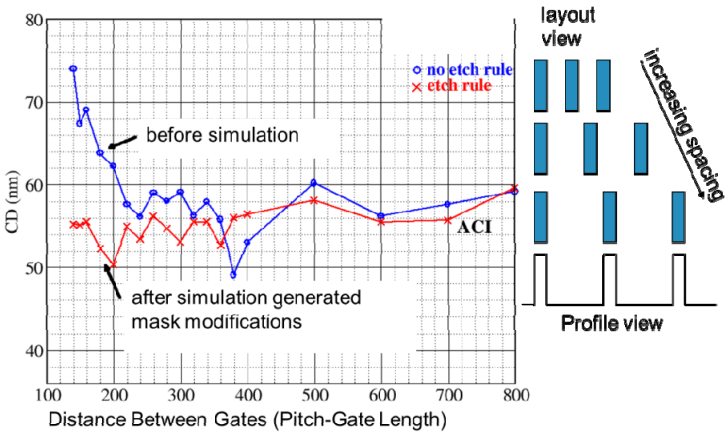

Figure 5. Predicted ACI with and without "simulation predicted" etch rules.

Computational patterning, from an etch and integration perspective from the late 2000's to the early 2010's retreated to the act of simulation engineers eking out suggestions from simulations and passing them through to process development teams. The absence of first principles models for plasma chemistry and plasma species-materials interactions were significant hindrances to the advancement of computational patterning with the introduction of new materials in logic devices.

3. BEYOND PATTERN TO PROFILE, SELECTIVITY AND DAMAGE

3.1 Integrated Simulations and Current Process Development

Up to this point the discussion with a few exceptions has revolved around CD prediction (ADI-ACI) largely driven by view factors, aspect ratio dependencies and loading. Producing structures in silicon materials meeting the electrical requirements of device designers is about managing profile and material property integrity (damage) and selectivity through the cascade of many process steps beyond optical development and mask fabrication. Predicting this via simulation is of immense value. OPC simulation is mainstream. But, "keeping it real," the concurrent or predictive use of simulation for integration involving plasma based unit processes has not been demonstrated; being generous, at the very least it is not pervasive. It has not been that effort has been lacking. In today's technology in high volume manufacturing, realizing the "virtual fab" is difficult because of the multi-physics nature of the bulk plasma and plasma-materials interactions part of the problem is very difficult.

3.2 Process Emulation for Profile Evolution

With decades of effort behind it, at least profile simulation is finding its way to the mainstream. With sparsely populated plasma chemistry and plasma-materials interactions databases predicting mask patterns and device structure evolution has come to involve process emulators with varying degree of detail. Including as much physics as possible but relying heavily on fitting, etch and deposition emulators have found their place in technology development. Emulators comprise

a means of coupling information about species flux and energy with a representation of how the species and energy will drive reactions on a surface and translate it. The flux and reaction information can be very detailed or not at all. Once fitted, emulators work well provided the process steps are continuous or are at quasi-steady-state. In surface science parlance, the reactions ought to be well described by a constant surface "coverage" throughout a process step. An example of process emulation is included in Dunn *et al*., [20] (Fig. 6) in which the patterning process through hard mask assembly was modeled using a particle Monte Carlo (PMC) feature scale model that incorporates surface

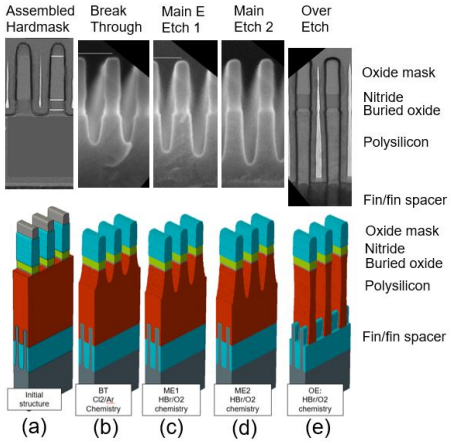

Figure 6. A montage of STEM, cross-section SEMs and simulated structures describing the transfer of a hardmask pattern through to the final polysilicon structure. (*Reprinted with permission from Proc. SPIE 10149, 101490Q (2017) [Copyright 2017], SPIE.*)

chemical reactions. Species and energy flux inputs to the PMC model were derived from simulations of the relevant etch chamber. Emulation with tight coupling to process experiments can be effective describing complex integrations. However, their application requires calibration. It is easy for unphysical mechanisms to enter an emulator limiting their extendibility outside the calibrated domain. This is important for development. In high volume manufacturing, should the processes and layouts not change significantly the risk associated with unphysical mechanisms is relatively small.

4. ATOMIC PRECISION PROCESSING

4.1 Temporally and Spatially Segregated Processes

Continuous plasma processes have gradually given way to pulsed plasma processes or spatially segregated plasmas for the fabrication of advanced devices.[21-24] Very simply, the dynamic range of radical species, ion species and energy available from a continuous plasma process is inadequate to manage the process trade-offs (damage/selectivity, ARDE, profile, uniformity) associated with their role at the substrate surface.

Pulse periods on the order of radical or by-product residence times tend to control passivation layer or polymer film thickness[22]; pulse periods on the order of ion species residence time and longer than the electron thermalization time control the radical to ion flux ratio and plasma chemistry.[22,23] Temporally segregated plasmas are effective at significantly lowering ion energies. These capabilities are needed to minimize damage and control profiles ideally to within an atomic thickness.[24]

In addition to the challenges of forming self-aligned contacts and double patterning, achieving successful FinFET fabrication at the 7 nm node brought the need of these capabilities to the fore. Retaining the fin oxide mask and iso-dense profile equivalence are critical for gate while retaining height with fin profile control (footer removal) is critical for fin construction. Process optimization taking advantage of flavors of pulsing technology permits the fabrication of advanced gate structures. Fig. 7 includes SEMS illustrating one such optimization.

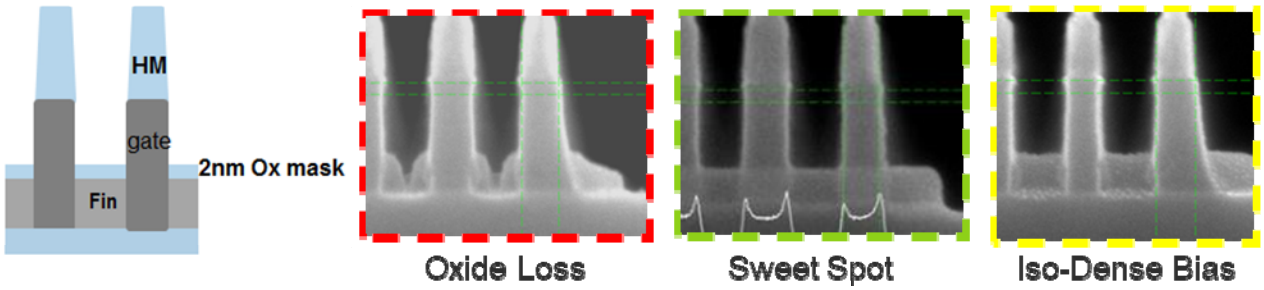

Figure 7. Optimization of a gate etch managing oxide loss and iso-dense bias.

Appreciated from this illustration is the pattern sensitivity of the process optimization. In this example, mitigating process bias is foremost a matter of managing the etch processes. Not only are pitches tight and critical widths thin (14 nm- 8 nm fin, 42 nm pitch; 10 nm – 7 nm fin, 34 nm pitch; 7 nm – 6 nm fin, 30 nm pitch)[25,26], 7 nm constitutes 30 atoms. At 5 and 3 nms, one atomic layer constitutes a significant variation. Challenges such as managing overlay error and variations due to line width roughness (LWR) will be compounded looking to 3 nm. Gate all around (GAA) FETs, nanowire/sheet FETs and new compound semiconductor materials promise to be introduced. Already "topographic" in nature, new 3D device fabrication will require isotropic processes to manufacture recesses in and around already printed structures. To begin these devices quadrupole patterning (SAQP) will almost certainly be required. The "patterning" requirements for starting SAQP and final 3D structures are that of "atomic precision." To achieve atomic precision, continuous plasma and pulsed plasma processes (etch and deposition alike) are now evolving to self-limited cyclic etch processes. This disruption in how patterns and devices are created merits a reconsideration of what computational patterning exactly means.

4.2 New Cyclic Processes: Self-Limitation and Chemistry Control at Surfaces

Self-limiting cyclic (etch and deposition) processes are far from new.[27, 28] Processes may be purely chemical in nature or plasma based. A common characteristic is alternating cycles of step 1) creating a reactive surface and step 2) removing that surface or using that surface as one primes for subsequent addition of new atoms. In atomic layer deposition, these are referred to as AB or ABC processes to denote the different kinds of process steps in a cycle. Ideally, the physical and chemical processes driven with species and energy flux from a gas, liquid or plasma stop when one atomic layer is converted. Variations of self-limiting cyclic etch and deposition processes decouple the optical patterning steps entirely from the process steps. Now, "biases" are a feature of the processes that can be introduced by fiat provided chemistry control is available on all surfaces of topographic structures at all times in any unit etch or deposition process. Digital etch and deposition processes with total chemistry control are selective area processes: selective area etch (SAE) and selective area deposition (SAD) or writ large selective area processing (SAP). "Ideal" self-limiting processes are immune from through pitch biases. View factor effects that lead to these bias are eliminated. This is the promise.

Were self-limiting processes available for the choosing (with chemistry control on every surface) computational patterning would become simple. Well-honed optical lithography models would predict the initial patterns and emulators calibrated for digital chemical processes on the surfaces would take care of the rest. Unfortunately, this ideality is physically unrealizable today. Starting surfaces are not pristine, underlying films are rarely crystalline or stoichiometric and the repeated removal and addition of atoms themselves leads to the production of defects. Process involving ions as a desorption medium will sense angle variations and energy variations across a wafer. Chemical processes on multi-material topographic structures poses an additional challenge. Unless processes are epitaxial in nature, it impossible to rip a monolayer from an ideal surface without leaving the remaining layer undisturbed. Any contaminant species will adhere to the virgin surface preventing it from reconstructing. Finally, SAP with isoptropy control on one surface without influencing another has not been demonstrated for the families of materials (*e.g.*, Si, SiO2, SiN, TiN) relevant to devices looking ahead to 3 nm.

5. COMPUTATIONAL PATTERNING: LOOKING FORWARD

5.1 First-Principles Simulations for Plasma Surface Interactions

This is not a pessimistic story for process development or device manufacturing. With the non-idealities that exist in atomic layer processing, the problem of managing process trade-offs remains but process margin is gained. Honda *et al*.

demonstrated that quasi-atomic layer etch process can be successfully leveraged.[29] Profile control is feasible even in non-ideal conditions provided limits are considered. Rastogi *et al.* also demonstrated this for a critical "bottom-up" patterning application.[30] From a computational patterning perspective, combined but decoupled optical patterning and emulator simulators are necessary. It means that high impact computational patterning constitutes concurrent simulations and process experiments that indicate how to process topographic structures to achieve device designers requirements once developed.[31]

An advantage exists now that was not present when initial efforts at virtual fab were conducted. The simulation of everything" lithography through process cognizant of chamber characteristics was not possible due to the massive nature of what needed to be computed. Feature and chamber scale models were very challenging; plasma surface interactions models were fits. First principles representations of how species generated in plasmas interacted with surfaces were virtually impossible. Computing sticking coefficients using first principles was tried but the effort not sustained.[32,33] Classical approaches were also tried.[34] Non-self-limiting processes have the facility that they modeled based on continuous experiments. Surfaces can be presumed to be in quasi-steady-state. Advances in computer power (at lower costs) and parallelization of first principle simulation software make fundamental calculations of important plasma surface interactions possible.

The fundamental advance making first principles simulations of plasma surface interactions tractable was the ability to simulate enough atoms to represent a surface. Gaussian density functional theory (DFT) methods, in which all system electrons are treated, are so computationally expensive that even today they are really only useful for small cluster calculations; they are therefore useful only for gas phase chemistry studies. Plane wave DFT is the emerging workhorse for engineering plasma surface interactions with atomic precision. Plane wave DFT, in which only the valence electrons are involved in the computation, facilitates the simulation of much larger systems. Often, when large halogens are involved in surface interactions, long range dispersion (London) forces are involved necessitating simulating a minimum 3 nm dimensions further necessitating the treatment of large slabs of atoms. Plane wave DFT has the disadvantage though of handling transition metals; a key advantage however is that ab-initio Monte Carlo is manageable for large systems and interactions can be visualized and explored through computational experiments. Important for plasma-surface interactions studies is the ability to handle excess electrons that are present when dielectric surfaces are charged.

5.2 Chemistry Control at Surfaces and Area Selectivity

A case study for the use of advanced computational methods for the purposes of patterning engineering is isotropy control in silicon nitride etching. A crucial aspect of self-aligned double patterning is etch of a silicon nitride film over a mandrel. The profile of the etched film is critical. Sherpa *et al.* discovered that hydrogen treatment followed by a fluorine-based *plasma* could be rendered isotropic with high-pressure plasmas (H radical dominated) and anisotropic with low-pressure plasma (H ion dominated).[35,36] In effect, the patterning is fully developed by plasma treatment making this an example of area selective etch. First principles simulations show how the hydrogen tends to bond with nitrogen's lone pair electrons which weakens the silicon – nitrogen bond making the silicon susceptible to fluorine attack. SEMs illustrating the process with companion first principles simulations are presented in Fig. 5. This process is quasi-self-limiting as the etch is limited by hydrogen transport which is diffusion dominated and anisotropic because of how the hydrogen is delivered to the surface.

Another approach to area selectivity is to use new or novel precursors that deliver the desired area selectivity. This is an active area of research today with the primary focus being on non-plasma approaches. Even in a plasma free environment it is challenging to invent precursors that selectively manipulate the "Si, SiO, SiN, SiC" system of materials on multi-color surfaces. The engineering around their incorporation and acceptance in manufacturing presents another challenge. Plasma process manipulation of surfaces to facilitate quasi-self-limiting chemistry for area selectivity is a paradigm shift in patterning and device fabrication technology and viable "work around" absent new precursors.

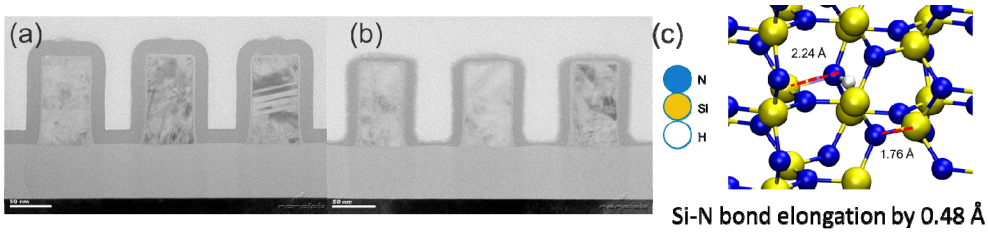

Figure 8. (a) An SEM of the starting silicon nitride over a mandrel; (b) SEM post hydrogen plasma treatment and fluorine plasma based etch; (c) a first principles simulation indicating the weaken of the silicon-nitrogen bond by hydrogen bonding to the nitrogen lone pair electrons. *((a) and (b) Reprinted with permission from J. Vac. Sci. Technol., A (35), 05C310 (2017) [Copyright 2004], American Vacuum Society.)*

6. OUTLOOK

To expect mature lithography models to bear the burden of predicting etch dependent patterning is unfair. It is difficult to imagine that the multi-physics "etch" can be predicted in its entirety by a single physics and chemistry based simulation suite. There are too many steps on too many materials involving too many plasma sources with too many chemistries. Pursuing advances in scaling, however, does not require this. Computational patterning is at a crossroads. Atomic precision processes, in theory, entirely decouple etch and deposition process topography results from optical development of a photoresist. Process emulators could capture the simple results of self-limited plasma etch and deposition processes and be used to alter photomasks for RIE lag free, iso-dense bias free and potentially damage free processes.

With ideal self-limiting plasma or thermal processes providing facile multi-surface chemistry control unavailable, the outlook computational patterning is bifurcated. Emulators have a place but the great new power of computation comes from today's ability to leverage first principles models to describe plasma surface interactions with ever-increasing fidelity. These can be used concurrently in process development to extract as much ideality as possible from quasi-self-limiting processes and invent new means of profile control. This is easy to state on paper. In fact, significantly more research is needed to realize the benefits of first principles models. First-principles models remain constrained by their ability to handle the large range of length and time scales pertinent to plasma surface interactions. For now, using first principles quantum chemistry models for nanometer order spatial scales and picosecond order time scales in tandem with kinetic Monte Carlo (KMC), classical molecular dynamics or continuum models is adequate. Hybrid approaches (*e.g.*, mixed quantum and classical molecular dynamics) are the way of the future but themselves require more development. These will be driven by the increasing importance of materials integrity, selectivity and profile in selective area processing.

Traditional large scale integrated lithography to feature scale and equipment models still have a place as even atomic layer etch and deposition processes involve process trade-offs. Metrology is a challenge that cannot be left without mention. While optical CD measurement is purported to be possible at the angstrom level, including compact models based on simulation of etch bias will be needed for profile estimation. In-line control will certainly require some combination of plasma diagnostics, compact models based on simulation or theory for their interpretation and intelligent systems for their training. Obtaining high fidelity feature construction at the atomic level will involve large scale simulations being tightly coupled to process experiments. Then, in the end, computational patterning becomes the act of computation, both first principles and large scale integrated multi-physics models, helping to guide the experiments of process engineers that do etch bias corrections: *etch aware computational lithography by experiment.*

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