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Introduction

The ninth topical conference on Photonics Packaging, Integration, and Interconnects was held at the San Jose Convention Center, 23-25 January 2007, as part of OPTO 2007 in conjunction with Photonics West 2007. This volume contains papers describing the material covered in the 28 presentations at the conference, which comprised 8 invited papers and 20 contributed papers. This volume also includes the papers presented at two joint sessions with the Opto-Electronic Integrated Circuits Conference on Optical Interconnects. Since the topic area of Optical Interconnects spans both conferences we, the Conference Chairs, decided to form two joint sessions on the topic so that attendees could benefit from the many presentations in this expanding field.

The conference was divided into six sessions spanning one-and-one-half days, plus two joint sessions with OEIC held on the Tuesday afternoon prior to the six sessions of Photonics Packaging. Including the joint sessions, three sessions were devoted to the topic of Optical Interconnects. One session focused on Fabrication and Advanced Materials for Packaging, one on Packaging/Assembly for Low-Cost Components, one on Components for Optical Instrumentation, one on High-Power Components and Thermal Issues, and one on Component and System Integration.

We experienced a 43% increase in the number of contributed papers in this conference over last year, with many new packaging and integration topics such as Optical Instrumentation, High-Power Components, and Low-Cost Packaging. We had a diverse range of papers from "High-power slab-coupled optical waveguide laser array packaging for beam combining," to "Novel cost-effective carbon nanotubes deposition technique using optical tweezer effect," and several papers on silicon photonics. Our speakers, also, represented a wide range of activities and geography: academia, industry, and private consultants, from North America, Europe, and the Pacific Rim. This year, we also had one speaker from Australia and two from Russia.

This past year has witnessed a new surge in photonics and, especially, photonics packaging. It has been an eventful year, including my transition to a new company as Director of Packaging. In a recent presentation by Michael Lebby, President and CEO of the Optoelectronic Industry Development Association, nearly every field utilizing photonic devices and components experienced significant growth in 2006. As I write this, the annual Consumer Electronics Show has just ended. Along with the many various new consumer products to debut this year, one drew exceptional interest — enough interest for an article in the *New York Times* on January 11. This was a scanning, laser-based "Pico" projector, small enough to fit within a typical handheld PDA. This subminiature projector could project a full-color video image about the size of a typical notebook

computer on any flat, near-white surface. Imagine the Photonics Packaging issues involved in this device.

As in 2006, OPTO 2007 and the other symposia held concurrently at Photonics West 2007 will be providing on-line access to the presented papers within a very few weeks through SPIE's Digital Library. The time from laboratory result to publication has never been shorter. Of course, the familiar Proceedings print volumes and CD-ROM versions also will become available following the conference.

I believe the reader will find that the enclosed papers are an excellent representation of the rapidly changing development in the packaging and integration of photonic and optoelectronic devices and systems and optical interconnects. The authors have done an outstanding job of presenting their impressive results at this year's conference.

Allen M. Earman
Ray T. Chen

Low-cost Micro-optics for PCB-level Photonic Interconnects

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ABSTRACT

One of the grand challenges in solving the interconnection bottlenecks at the Printed Circuit Board (PCB) and Multi-Chip-Module (MCM) level, is to adequately replace the PCB and intra-MCM galvanic interconnects with high-performance, low-cost, compact and reliable micro-photonic alternatives. Therefore we address the following components in this paper: 1) out-of-plane couplers for optical waveguides embedded in PCB, 2) peripheral fiber ribbons and two-dimensional single- and multimode fiber connectors for high-speed parallel optical connections, and 3) intra-MCM level optical interconnections via free-space optical modules.

For the fabrication of these micro-optical interconnect modules, we are focusing at the Vrije Universiteit Brussel on the continuous development of a rapid prototyping technology, which we call Deep Proton Writing (DPW). The special feature of this prototyping technology is that it is compatible with commercial low-cost mass replication techniques such as micro injection moulding and hot embossing. Laser ablation is used at Ghent University for the fabrication of PCB-embedded waveguides and integrated micro-mirrors. The main advantage of this technology is that it is compatible with present-day PCB manufacturing.

For the free-space MCM-level optical interconnect module, we furthermore give special attention to the optical tolerancing and the opto-mechanical integration of the components. We use both a sensitivity analysis to misalignment errors and Monte Carlo simulations. It is our aim to investigate the whole component integration chain from the optoelectronic device to the micro-opto-mechanical components constituting the interconnect module.

Keywords: deep proton writing (DPW), fiber connectors, laser ablation, micro-optics, optical interconnections, out-of-plane coupling, polymer multimode waveguides, replication techniques

1. INTRODUCTION

High-speed data links between digital processing units are currently under high pressure. It is indeed not unusual for present-day galvanic multi-gigabyte links to require compensation on the high-frequency components for as much as 20 to 30dB of attenuation, while cross-talk, dispersion and timing issues become more severe with each newly introduced CMOS technology node. As a consequence present-day high-speed links already show an extraordinary complexity, use a large part of the chip's real estate and are responsible for a considerable part of the power consumption.

In the meanwhile, Moore's law is relentlessly fulfilling its prophecy: with each generation we are able to integrate more and faster transistors on a given chip's surface. The performance of galvanic interconnects, on the contrary, is not advancing with the same pace. This has led to a long predicted and overwhelming interconnect bottleneck between an abundant local computing power on the local transistor networks and the imbalanced interconnect capabilities on higher physical and hierarchical levels. Note that the technique of further

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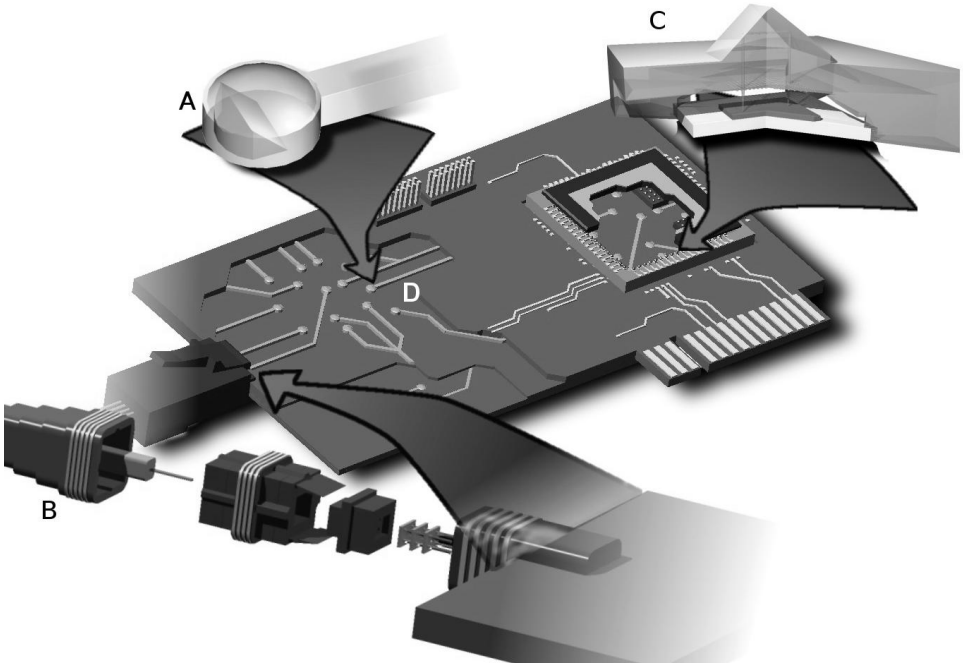

Figure 1. Examples of micro-optical components for board-level photonic interconnects.

parallelizing the number of connections between chips is also running out of steam since the current pin densities do not scale any more due to a worsened signal integrity and packaging costs.

One way to alleviate this technological deadlock is to radically change the interconnect technology. An often cited and promising approach is to make extensive use of photonic interconnections. Indeed, optics as a wire replacing technology has some clear physical reasons for its superior interconnect characteristics as compared to its galvanic contenders.[1] Optical interconnects have already demonstrated their ability to enable data transmission at very high-bit rates per channel and this almost independently of distance. The immunity to electronagnetic interference and the potential of lower power consumption are additional assets.

Since the introduction of the concept of using optics as a wire replacing technology, a large body of work has been dedicated to comparing the benefits and limitations of optical versus galvanic interconnections.[1–3] Typically, a "break-even length" is defined above which optical interconnects are preferred from a performance or power dissipation point of view. Although this length varies substantially with technological assumptions, a clear trend has been set: the level of system hierarchy where optical interconnects show clear advantages over electrical interconnects becomes distinctly lower.

If we want to solve the interconnection bottlenecks at the Printed Circuit Board- (PCB) and Multi-Chip-Module- (MCM) level one of the grand challenges for the next five to ten years is to adequately replace the PCB and intra-MCM level galvanic interconnects with high-performance, low-cost, compact and reliable micro-optical and micro-photonic alternatives. Such an optically enhanced interconnect approach should allow to seamlessly extend the optical fiber data path to the very heart of the data-processing chips using e.g. polymeric waveguides, free-space refractive, diffractive or hybrid plastic micro-optical components or a combination thereof. In the long run one even considers to deploy photonic integrated circuits, featuring nano-sized photonic bandgap waveguides. However, these approaches can only prove their worth in practical and economical viable real world systems if they can be made compatible with low-cost mass fabrication technologies and standard semiconductor packaging techniques.

Today a variety of technologies exist that make it possible to embed polymer-based optical waveguides in standard FR4 printed circuit boards, such as UV exposure,[4] laser direct writing, embossing[5] or laser ablation.[6]

These optical waveguides are schematically illustrated in figure 1(D). Recently, increasing emphasis in PCB-integrated waveguide technology is placed on the use of multilayer optical structures where each optical layer contains arrays of multimode waveguides and other passive optical elements. This is driven by the availability of 2-D arrays of pto-electronic elements such as VCSEL- and photodetector arrays. The use of multilayer structures additionally allows to considerably increase the integration density and to simplify the routing schemes. However, the above solution requires the development of a new class of micro-optical structures, which are designed to extract optical signals from these waveguides (or from one layer to another) and efficiently couple them with optoelectronic components that are mounted on the PCB. A common approach is the use of 45° micro-mirrors. Various techniques are being applied for the fabrication of these micro-mirrors. Reactive ion etching,[7] diamond blade cutting[8] and laser ablation[9] allow the formation of micro-mirrors in the waveguide itself. Using Deep Proton Writing (DPW)[10] we fabricate a free-standing, pluggable out-of-plane coupler, designed to fit into a laser-ablated cavity that gives access to the polymer optical waveguides embedded in the printed circuit board. It features a 45° angled facet that bends light from an embedded optical waveguide upward via total internal reflection, as illustrated in figure 1(A). Another interfacing component that we have designed to overcome the remaining micro-optical hurdles to massively introduce photonic interconnects in digital systems, exists of peripheral fiber ribbons and two dimensional single- and multimode fiber connectors for high-speed parallel optical connections shown in figure 1(B).

At the MCM-level, density arguments can require free-space micro-optical interconnections. Our approach here is based on a micro-prism reflector which transports and routes data-carrying light beams from a micro-emitter to a micro-detector array, hence bridging intra-chip or chip-to-chip throws ranging between a few tens of millimeters down to only a few millimeters (see figure 1(C)). The development of a packaging solution for both the optical interconnect level as well as the electrical interconnect level is a key requirement to enable the successful introduction of optics at the intra-MCM level. We show that it is possible to integrate free-space micro-optical modules with electro-optical devices by integrating a Low Temperature Co-fired Ceramic (LTCC) intermediate wire carrier with a mass-fabrication compatible spacer structure fabricated with DPW. The DPW spacer is a part of the opto-mechanical packaging and provides the necessary features to align the optical baseplate on top of the chip using micro-spheres and visual alignment marks. The LTCC in its turn is a part of the electrical packaging and shortens the bonding loops from chip to package, ensuring enough height clearance above the optoelectronic chip to allow the desired working distance of the micro-optics with respect to the active area of the chip.

In what follows we will briefly touch upon the functionality and the present-day experimental characteristics of these different board-level interconnect components, as well as give a short description of the fabrication technologies used, i.e. laser ablation and deep proton writing.

2. PRINTED CIRCUIT BOARD EMBEBBED WAVEGUIDES

Various research groups all over the world have explored different optical systems to create densely packed photonic interconnects. An early popular approach for optical interconnect demonstration was the use of free-space optical links combined with macro-optics.[11, 12] For this approach, the use of stainless steel slotted baseplates with components centered in steel cells[13] proved to be a very flexible and robust interconnect prototyping technology capable of creating a massive number of parallel interconnects by aligning just a few components.[14, 15] Such systems are however only practical in laboratory setups, primarily because of their high weight and large size constraints. A promising alternative for parallel free space optical interconnects is the use of planar optics modules. These Planar Integrated Free Space Optical (PIFSO) modules are developed by the University of Hagen and fold a free space optical system inside a thin glass substrate.[16] It provides the benefits of free-space optical systems in providing high channel count densities without much of the alignment and stability problems of the other approaches. The biggest challenge in this approach is to create a communication channel with high link efficiencies by adopting highly efficient diffractive optical elements.

Other approaches for creating practical optical interconnects are using beam-guiding techniques which constitute of individual fibers,[17] fiber ribbons[18] or even fiber imaging bundles.[19] One technique that has recently gained lot of attention is to embed waveguides into standard FR4 printed circuit boards.[20] The decision to

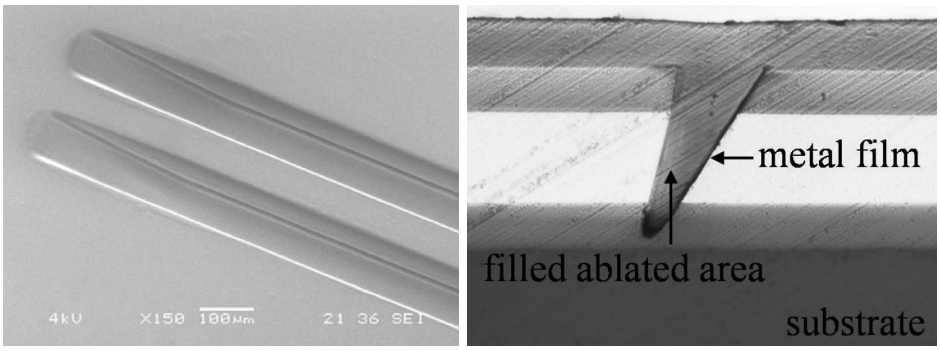

Figure 2. Left: SEM picture of a KrF laser ablated multimode polymer waveguide. Right: Cross-section of a metallized laser ablated 45° micro-mirror.

commercially implement one or more of the optical interconnect approaches highly depends on the ease of integration in standard semiconductor packaging and compatiblity with low-cost mass fabrication technologies. One attractive technology to fabricate these PCB-embedded waveguides is laser ablation, as used at Ghent University.

2.1. Laser Ablation

Laser ablation is a flexible non-contact micro-machining technology that can be used to structure a large variety of materials.[6] It is a mask-less technology making it extremely useful for fast prototyping of a wide variety of polymers. Moreover, one of its main assets is that it is fully compatible with present-day PCB manufacturing, since it is already used for the drilling of micro-vias into high-density boards. Laser ablation can be described as a micromachining technology based on the controlled removal of material using intense laser pulses. In general, the energy of the laser beam is absorbed in a thin layer or a small volume and the ablation process takes place through rapid defragmentation. Depending on the material, this can have the characteristics of ablative photodecomposition, or rapid heating and vaporization. KrF excimer laser ablation (wavelength 248nm) is particularly well suited for the structuring of polymers because of their excellent UV-absorption properties and highly non-thermal ablation behaviour. Two commercially available materials are currently being investigated for patterning with laser ablation: Truemode Backplane polymer, a highly cross-linked acrylate-based material and Epocore/Epoclad, an epoxy-based material. Besides their excellent optical properties, both materials exhibit excellent thermal and environmental properties and are fully compatible with present-day PCB manufacturing and soldering processes. Since the laser beam can be tilted, it allows the fabrication of integrated micro-mirrors for the coupling of light in and out of the waveguides at the desired locations. The sample to be patterned is positioned on computer-controlled high accuracy translation stage with a $1\mu m$ motion resolution.

2.2. Multilayer waveguides and integrated coupling structures

The optical layer integrated on a PCB is generally built up as a cladding-core-cladding stack, where the cladding has a slightly lower index of refraction than the core material. Multimode step-index waveguides are most likely to be used on PCBs since their dimensions (in the order of $50\mu m \times 50\mu m$) do not require an extremely high alignment precision and intermodal dispersion will not be an issue since the targeted distances to be bridged are relatively short. To create a waveguide in the core layer, material is removed by laser ablation on both sides of the resulting waveguide, shown in the left part of figure 2. Average propagation losses of laser ablated Truemode waveguides were measured to be 0.13dB/cm at 850nm using a cut-back method.[6]

Nowadays, emphasis is shifting towards multilayer optical waveguides, allowing for a significant increase in integration density and a better compatibility with 2-D optoelectronic VCSEL- and photodetector arrays. Furthermore, it offers possibilities towards complex routing schemes by switching between layers using micro-mirrors. A cross-section of a metallized ablated micro-mirror can be seen in figure 2. The alignment accuracy between the optical elements in the different layers requires special attention in view of the impact on the overall system efficiency. The angle accuracy of a laser ablated micro-mirror is $\pm 1°$, whereas the alignment accuracy between two optical layers is smaller than $5\mu m$.[21] An example of a laser-ablated multilayer waveguide structure on FR4 substrate, with integrated micro-mirrors is shown in figure 3.

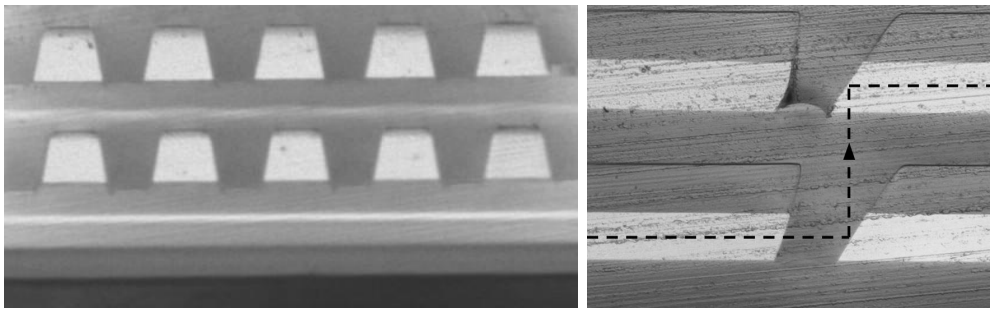

Figure 3. Left: Two-layer PCB-integrated waveguide structure ablated in Truemode Backplane material. Right: Cross-section of an inter-plane coupling mirror configuration, where light undergoes a double 90° bend with conservation of the propagation direction.

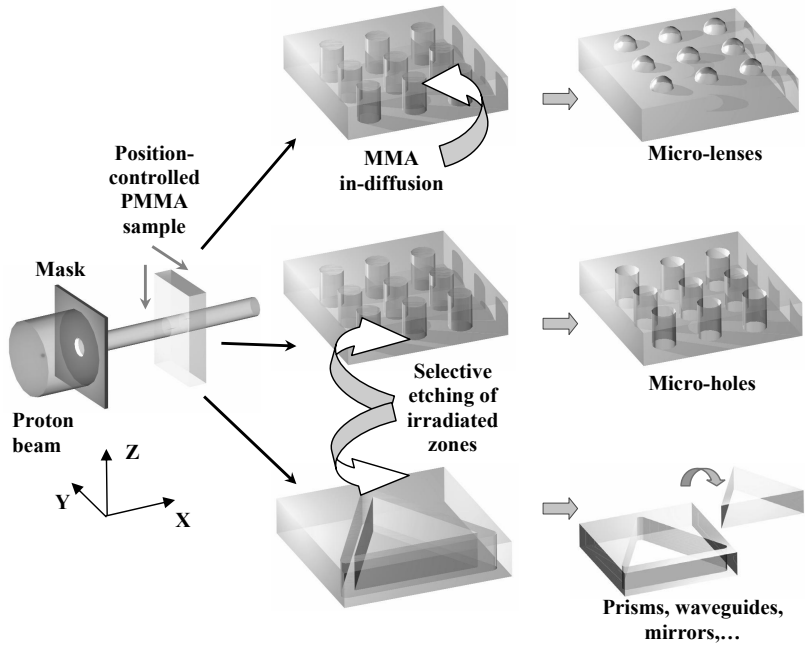

Figure 4. Deep Proton Writing: basic processing steps. After a patterned irradiation we can either apply a binary chemical etching to remove the irradiated regions or we can in-diffuse a monomer vapor to create micro-lenses through a swelling process.

3. MICRO-OPTICAL INTERFACING COMPONENTS FOR BOARD-LEVEL INTERCONNECTS

3.1. Deep Proton Writing

At the Vrije Universiteit Brussel, we are optimizing a dedicated technology, named *Deep Proton Writing* (DPW). Its concept finds its origin in the LIGA-technology[22] but differs on two important aspects. First, it is based on the use of protons rather than electromagnetic X-ray irradiation to shape polymer samples. Secondly, the DPW technology is using a direct write methodology as opposed to the projection lithography which is adopted for the LIGA-process where expensive masks are required for each new LIGA design. In fact, the thick masks required in the LIGA process are made in steps by repeating the LIGA process with a gradually higher energy until a mask with sufficient thickness can be electroplated. Both differences make that the DPW process requires less infrastructural demands and has the potential of being a more flexible technology for rapid prototyping.

The basic concept of the deep proton writing process is based on the fact that irradiating swift protons onto

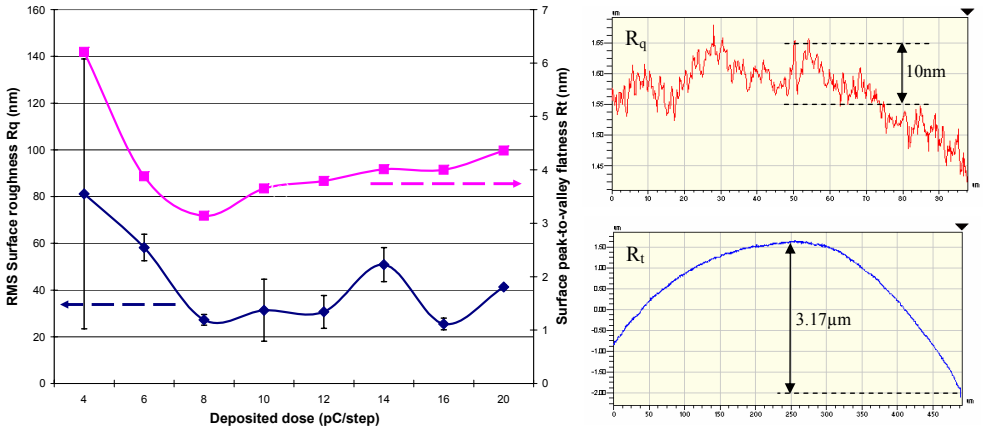

Figure 5. Left: Surface roughness R_q and flatness R_t as a function of deposited charge per $0.5\mu m$ step during irradiation. Right: Detailed plots for R_q and R_t at the charge collection of 8pC per step of 500nm.

a poly methyl methacrylate (PMMA) sample featuring linear polymer chains (i.e. opposite of crosslinked) of high molecular mass, will rupture the long chains. As a consequence, the molar mass of the irradiated material will be reduced and free radicals will be created in the polymer, resulting in material properties that are very different from those of unexposed material. Two different chemical steps were developed that can be applied to the proton bombarded areas. The first consists of etching the exposed area with a specific developer to produce micro-holes, micro-mirrors and micro-mechanical structures. The second process involves the in-diffusion of a MMA monomer to locally swell the irradiated zones. This will result in micro-spherical and micro-cylindrical lens surfaces (see figure 4). Both processes can be applied to the same sample after a single irradiation session as the dose required for etching or for swelling is very different.

For the etching process, we make use of a GG developer (diethylene glycol monobutyl ether 60%, morpholine 20%, 2-aminoethanol 5%, and DI water 15%) as the etching solvent. For standard components, etching lasts 1 hour at an elevated temperature of 38°C. During the whole process the etching mixture is stirred by an ultrasonic stirrer. The etching is stopped by dipping the component in a stopping bath consisting of 20% water and 80% diethylene glycol monobutyl ether. Recently, we have optimized the surface quality of the etched surface after irradiation with the smallest aperture of $20\mu m$ in our final collimation mask. With this proton beam size, an error in the postion of the beam will be more pronounced and the signal-to-noise ratio of the measured proton current will be significantly smaller than with our standard $140\mu m$ proton beam (as the proton current is 49 times smaller to obtain an equal proton fluence). Nevertheless, we succeeded in creating very high quality surface profiles even with this aperture.[25] In figure 5, the resulting local surface RMS roughness (R_q) and peak-to-valley flatness (R_t) are given. The graph shows the surface R_q and R_t as a function of the deposited particle charge per step of $0.5\mu m$. R_t was measured over a length of $500\mu m$ along the proton trajectory and R_q was calculated by averaging several measurements over an area of $46\mu m \times 60\mu m$ with a non-contact optical profiler (WYKO NT2000). From this graph, we can conclude that the best results are obtained when we irradiate the sample with a collected proton charge of 8pC per step of 500nm corresponding to a peak proton fluence of 6.4×10^6 particles per μm^2. Figure 5 also shows the profiles of the created surfaces. On the bottom graph the profile is shown in the direction of proton trajectory with a surface flatness R_t of $3.17\mu m$. The top graph is a zoomed in version of a profile perpendicular to the proton trajectory. The RMS roughness R_q interval of 27.5nm is indicated on the graph as well. These results are on par with the surface roughness and the flatness results we are obtaining with larger apertures at the same entrance energies.

It is obvious that with a total cycle time of about half a day per component and the required accelaration facilities, the DPW technology cannot be regarded as a mass fabrication technology as such. However, one of its assets is that it can be made compatible with low-cost replication techniques. Indeed, once the master component has been prototyped with DPW, a metal mould can be generated from the master by applying electroplating. After removal of the master, this metal mould can be used as a shim in a final micro-injection molding or hot

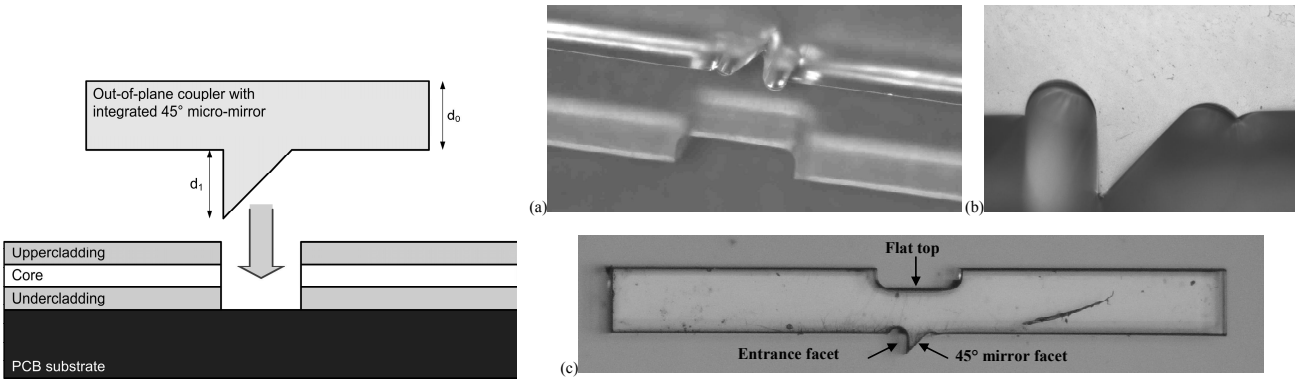

Figure 6. Left: Cross-sectional schematic of the use of a pluggable component with a 45° micro-mirror to realize out-of-plane coupling of light propagating in waveguides integrated on a printed circuit board. Right: DPW fabricated prototype of a branching waveguide with one out-of-plane coupling micro-mirror: overview (a), zoom on micro-mirror and tapered end facet (b) and zoom on micro-mirror (c).

embossing step.[23]

3.2. Out-of-plane couplers and optical tap waveguides

As cited earlier, one of the remaining hurdles for massively deploying PCB-integrated optical interconnect waveguides is to efficiently couple light in and out of the waveguides. In order to connect the optical signals to surface-mounted optoelectronic components, a 90° turn is required which can be accomplished either electrically or optically. The electrical turn is conventionally introduced by an extra small flexible printed circuit board while the optical 90° turn is conventionally accomplished by a 45° micro-mirror. Various techniques exist today to fabricate such angled facets on the embedded waveguides, as explained in section 1. The example of laser ablation for the creation of micro-mirrors directly integrated in the waveguides was detailed in section 2.1. Our concept presented here differs from most approaches since we propose a pluggable out-of-planing coupling component[24] instead of writing the micro-mirrors directly in the waveguides. We believe such components can be easily mass-replicated from a master prototype. The replicated components can then readily be inserted in laser ablated cavities on the printed circuit board to couple the light from the waveguide. The micro-mirror can either use total internal reflection or a metal coating to bend the light over 90°.

For the fabrication of this DPW component, we have chosen to use a proton beam collimating aperture of $125\mu m$, which causes some rounding in the corners of the component, as shown on the left right of figure 6, but this does not affect its optical functionality in any way. The design is such that once the component is plugged in, the micro-mirrors will reach $140\mu m$ under the PCB surface. Non-sequential optical ray tracing predicts that when the component will be plugged into a board with $50\mu m \times 50\mu m$ waveguides and with a numerical aperture (NA) of 0.3, the coupling efficiency will be 73% (-1.37dB). By using a metal coating over the micro-mirror, this efficiency can be further increased to 92% (-0.36dB). When testing the component directly (without the PCB waveguides) with multi-mode fibers at the entrance and the exit facet, we measure a maximal experimental coupling efficiency of 47.5% (-3.25dB). This is in good agreement with a simulated efficiency for this configuration of 63.4% (-1.98dB) considering the fact that we did not take scattering losses due to surface roughness into account for the simulations. The measured coupling efficiency increases to 56.5% (-2.49dB) if we apply index matching gel between the exit facet of the source MMF and the entrance facet of the out-of-plane coupler.

Another component we present here is an optical tap waveguide which realizes a 1-to-3 splitting of an optical signal through integrated 45° micro-mirrors, enabling for example the splitting of the output of an optical fiber equally into multimode waveguides integrated in a Printed Circuit Board (PCB) or the coupling of light to and from surface-mounted optoelectronic devices. This type of component would enable a seamless integration of the different optical interconnect approaches used on PCB-level.[25] For the fabrication of this branching waveguide, two different proton beam sizes are used during one irradiation and a $20\mu m$ collimating aperture is

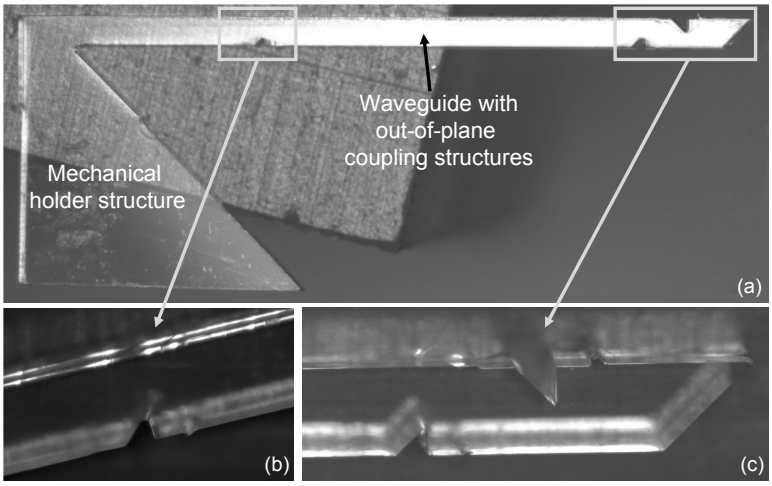

Figure 7. DPW fabricated prototype of a branching waveguide with three out-of-plane branching micro-mirrors.

chosen to accurately define the out-of-plane coupling micro-mirrors integrated in the branching waveguide. A fabricated prototype is shown in Fig. 7. Using a WYKO NT-2000 non-contact optical profiler (Veeco), we have measured the geometrical dimensions of these integrated micro-mirrors, resulting in depths of $120\mu m$, $150\mu m$ and $215\mu m$ for respectively the first, second and third micro-mirror shown in Fig.7. These measured values are all in close correspondence to the designed values of $123\mu m$, $155\mu m$ and $212\mu m$, indicating that we have successfully compensated the proton beam pointing misalignment when switching collimation aperture during the irradiation step. Due to the finite size and the circular shape of the proton beam, we observe some rounding at the bottom of the integrated mirco-mirrors. Feedback into the simulation software reveals that this rounding leads to a negligible amount of scattering visible as a broadening of the far field intensity profile. When measuring the optical coupling efficiency of each of the integrated branching micro-mirrors of the optical tap waveguide, we observe that the power coupled out by each micro-mirror is respectively 22.7%, 21.8% and 21.8%, which is in close correspondence with the targeted value of 20% during the design of the component.

3.3. High-density 2-D fiber connectors

High-precision two dimensional fiber alignment modules can offer large benefits for high-density photonic interconnects at the board-to-board and chip-to-chip level, where parallel light signals have to be transferred between integrated dense 2-D emitter and detector arrays. Even for the telecommunication infrastructure, the availability of highly accurate, low cost, field installable two dimensional fiber couplers would boost the further integration of fiber-optics in future fiber-to-the-home networks.[26] Using DPW, we prototyped a 2-D connector for single mode fibers that can be mass-fabricated with the required high accuracies and at low cost manufacturing. It features conically shaped micro-holes to ease the insertion of fibers from the backside of the fiber holder into sub-micron precision holes. The conical shape of the holes has been obtained by taking advantage of the ion-ion scattering effect of protons. This effect becomes pronounced when proton fluence is chosen in excess of 10^7 particles per μm^2. The optimized micro-holes for fiber-insertion feature a front side diameter of $134\mu m$, and inner diameter snap-fitting a fiber with cladding diameter specification of $125\pm0.7\mu m$ and a back side diameter of $165\mu m$. A schematic view of the obtained microholes can be viewed in figure 8.

The connector plate features a 4×8 array of holes with a pitch of $250\mu m$. Using the DPW technology we are capable of integrating alignment holes into the design during one single irradiation step. The fabricated alignment holes are two larger holes with a diameter of $700\mu m$, compatible with standard MT-ferrule pins. By measuring the rim of the micro-holes with an optical profiler we find a standard deviation on the hole positions below $0.8\mu m$ (limited by the measurement apparatus). Although the conical holes allow for a tight control of the lateral postion of the fibers, they still leave some angular freedom to the fibers. Therefore, we have opted to include in the DPW connector an additional mechanical pre-alignment plate, separated about 5mm from the

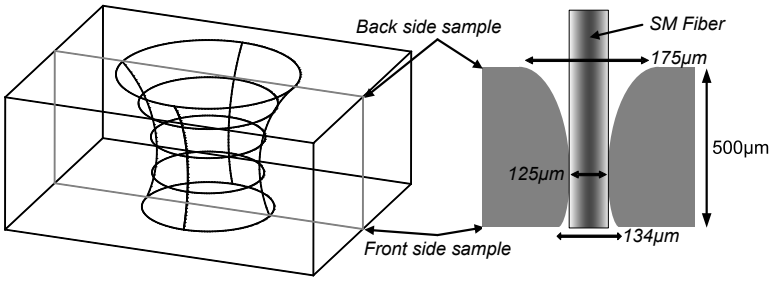

Figure 8. Schematic representation of the conical profile of the micro-holes allowing an easy fiber insertion from the back side.

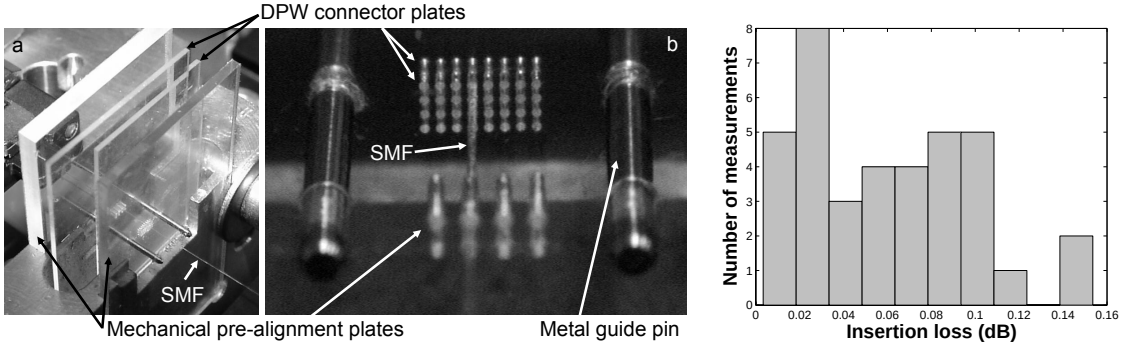

Figure 9. Left: The assembled 2-D single mode fiber (SMF) connector component in the setup for insertion loss measurements: Two pre-alignment plates for mechanical stability and two DPW connector plates with micro-holes are aligned using metal MT guide pins. Right: A histogram of the resulting in-line fiber-to-fiber coupling efficiencies.

DPW plate, as illustrated in figure 9. With this component, we measured an average in-line coupling loss of 0.06dB in the telecom C and L bands. The maximum coupling loss over 37 link experiments was 0.15dB.[27] The histogram of the connector losses over the whole array is shown in the right-hand side of Figure 9.

3.4. Intra-MCM optical interconnect module

Density arguments can require free-space micro-optical interconnections at the intra-MCM interconnect level. Our approach here is based on a micro-prism reflector which transports and routes data-carrying light beams from a micro-emitter to a micro-detector array, hence bridging intra-chip throws ranging between a few tens of millimeters to only a few millimeters. Such components emphasize the need for real three dimensional micro-optical modules. On its way from source to detector, each of the multiple beams are collimated, bended at the 45° angled facets and refocused by micro-lenses (see figure 10). We have shown that this type of interconnect modules has the potential to provide the highly desirable massive parallel high-speed interconnects needed for future generations intra-MCM level interconnections.[28] We are currently working towards a massively parallel intra-chip interconnect demonstrator that will carry a channel density above 4000 channels per cm^2 and hence provide us with low-cost, chip compatible, plug-and play, commercially viable interconnect solutions.[29] We are not only looking at the fabrication of the module, but we are also investigating how the component can be reliably attached above a dense optoelectronic chip. We have therefore developed a solution consisting of a spacer plate surrounding accurately the optoelectronic chip. The spacer plate and the optical interconnection module are aligned with respect to each other using precise micro-spheres. The various fabrication and alignment errors are further explained in section 4.

4. TOLERANCING STUDY OF THE INTRA-MCM INTERCONNECT MODULE

To ensure the manufacturability of the micro-optical and opto-mechanical devices, a plethora of requirements should be considered to ensure the necessary production ease, assembly speed, quality and reliability. The

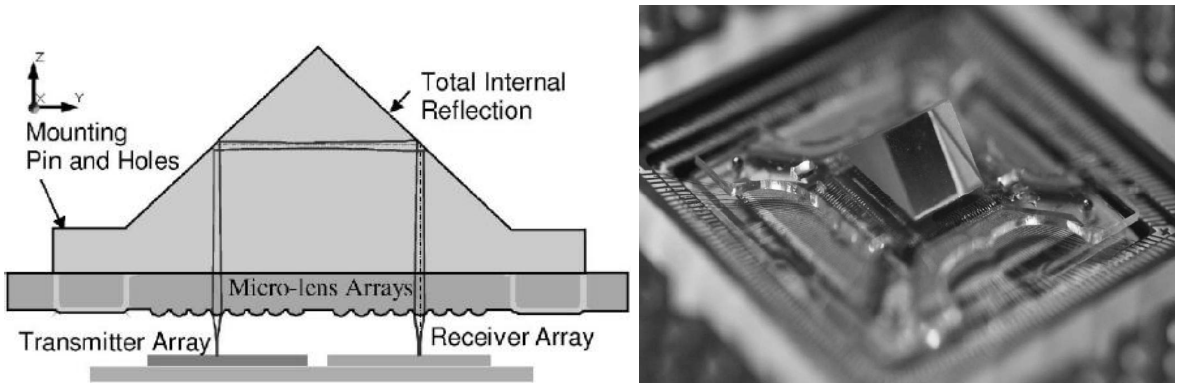

Figure 10. Left: Schematic representation of the free-space optical interconnect module. The optical beam path through the component is indicated. Right: Prototype of the demonstrator. Two of the four micro-spheres for alignment are clearly visible.

definition of an adequate set of tolerances for dimensional and geometrical errors is directly related to all the aspects of the Design for Manufacturability (DFM) process. Too tight tolerances will lead to costly production methods, difficult assembly and high fall-out of finalized devices, adversely affecting the total cost and time-to-market. Quality and reliability on the other hand are harmed by too loosely toleranced systems. Applying DFM principles on micro-opto-mechanical components is therefore key to achieve successful implementation of optics in digital data processing systems.

The challenge taken is to define a set of tolerances for the intra MCM interconnection module presented in section 3.4 and in figure 10 using a combination of optical simulations and geometry calculations based on the Monte Carlo method.[30] Full-scale link simulators[31] and smart-pixel packaging schemes have been reported in literature but in general none of these efforts have dealt with the specific tolerance problems arising in a realistic packaging scheme for free-space intra-chip optical interconnects. Although some optical simulation tools already provide an interface for tolerancing, this is usually limited to the core of the optical structure, and not the underlying mechanical alignment features.

We implemented the optical model using ZEMAX®. The modeling is based on non-sequential tracing of rays emitted in a Gaussian pattern with a given angular distribution Full Width Half Maximum (FWHM). These rays are traced through the collimating lens, reflected at the prism sidewalls by total internal reflection towards the focusing lens, where they are focused onto a flat, isotropic detector with a square surface of $20\times20\ \mu m^2$. The data returned from the optical simulation tool contains the light transmission efficiency in the data channel, and the stray light impinging on 4 neighbouring detectors causing cross-talk. The lens pitch was set to $220\mu m$ and the lens diameter to $125\mu m$ enabling the highest interconnect density with the current state-of-the-art DPW lens fabrication process. For the estimated 17.5° FWHM of the envisaged demonstrator, the nominal design was set to a focal length of $297\mu m$ at a working distance between chip and module of $270\mu m$, resulting in a -1.3dB transmission loss.[33]

4.1. Sensitivity Analysis

We have now perturbed the nominal design with errors of 11 different parameters to get insight into the prototyping and assembly yield of our fabrication process. The errors stem from translational and rotational misalignments of both the lens base plate and the prism within the interconnection module. We run a script to perturb the geometry of the module in a Monte Carlo manner using MATLAB®. The system can subsequently be simulated with the non-sequential ray tracer (ZEMAX®).

First, we performed a sensitivity analysis. In such a study, only one parameter is varied around the nominal value while leaving the other perturbations fixed to zero. We have observed that the translation of the complete module along the interconnect channel, and the rotation of the complete module around the vertical axis are among the most critical parameters. Next, we studied the effect when many misalignment errors are

Table 1. Main DPW technology specifications at $1\times\sigma$.

Parameter	Obtained accuracy	Remarks
DPW technology		
Position error	0.5 μm	Repeatable
Hole diameter	1.8 μm	Repeatable
Lens focal length	0.31 μm	Repeatable
Packaging		
Micro-sphere position	1.0 μm	Deformations
Working distance	3.0 μm	DPW system
Tilt errors	0.250°	Worst case
Adhesive layer	10 μm	To be confirmed

combined simultaneously. In this method a large batch of systems is simulated, each with a slightly different set of misalignments errors. The misalignments errors in each system are chosen randomly following a given probability distribution around the nominal value. When the effect of different errors is combined, the penalty for misalignment is further increased. For example, when all 11 parameters are perturbed with a Gaussian error with a standard deviation that is equal one third of each sensitivity interval*, the fabrication and assembly yield drops to 60%.[33]

4.2. Technology Constraints of the DPW technology

It is not only sufficient to look at the effect of combined geometrical errors. It would also be interesting know which specification of the DPW technology is the most important to ensure a high yield of micro-optical components. We now briefly explain the statistics of the fabrication errors that occur with our rapid prototyping technology.

Our previously described in-house technology of DPW is able to produce high-aspect ratio components in polymer, in which we rely on the accuracy of an XY-translation stage system (50nm closed loop) for sample positioning and the dose measurement system. A factor that is affecting the position accuracy and edge straightness are small variations of the proton beam impinging on the sample. These are caused by instabilities of the complete cyclotron beam-line and are believed to be larger than the translation stage error. We routinely see a surface flatness of $1\mu m$ (3.75mm scan length) or better, while micro-holes have a standard deviation of $1.8\mu m$ on their diameter (measured at the front of the sample). We also produce micro-lenses on the same substrate in one irradiation step. Positional accuracies and circularity of the lens footprints are thus similar to those found with micro-holes. The remaining parameter that controls the shape of the micro-lenses is the deposited dose. The relationship between the focal length of the micro-lenses and the dose has been documented in extenso[32] and DPW lenses show a focal length standard deviation of $0.31\mu m$ with a predominantly Gaussian shape. An overview of the main DPW technology specifications is given in table 1.

4.3. 3D geometrical modelling

The sensitivity limits and Monte Carlo analysis of Section 4.1 allowed us to draw conclusions on the most critical parameters and the effect of combined misalignments. The technique however suffers from two drawbacks. Real world technology accuracies do not scale uniformly. Secondly, the technique that was used did not follow the complete assembly chain, and did not include positional and rotational errors due to the package construction.

We were able to create a polygon-driven geometrical model in which all prototyping and assembly imperfections that occur with our accurate rapid protoyping technology as explained in section 4.2 are taken into account.[33] This fully fledged Monte Carlo simulation shows that the packaging solution which includes the

*The sensitivity interval is defined by the range for which one parameter can be altered before the component will be rejected due a drop in link efficiency or a too high a cross talk

micro-holes and micro-spheres to mount the interconnection module above the optoelectronic chip is a viable solution. With the combined optomechanical simulation we show that our DPW technology in itself is capable of handling the strict requirements set for the interconnection module (with a 91% chance of a link efficiency that is -0.75dB lower than the theoretical maximum), but the tilt and rotation errors caused by the adhesive bonding of spacer plate and the optoelectronic chip deteriorate the yield considerably to 25% even if we allow for an extra loss of -3dB.

5. CONCLUSION

We have given an overview of components paving the way towards low-cost printed circuit board-level optical interconnects. Laser Ablation was presented as a suitable technology to fabricate PCB-integrated optical waveguides, which can include multilayer stacks for higher interconnection densities, and integrated coupling micro-mirrors. To interface these PCB-embedded waveguides with fiber optics or 2-D optoelectronic arrays of VCSELs or photodetectors, we presented Deep Proton Writing as a rapid prototyping technology that can be made fully compatible with low-cost mass-fabrication. Some examples of these interfacing components were presented. A first component consisted of a two dimensional (single mode) fiber array connector, with coupling losses below 0.15dB. A second component was a pluggable out-of-plane coupling element that can be readily inserted into cavities in printed circuit boards to couple light to and from the embedded optical waveguides. A third component consisted of an optical tap waveguide with integrated 45° micro-mirrors for the 1-to-3 splitting of an optical signal. A fourth and final component targeted a free-space intra-MCM optical interconnection. For this component, we presented also the typical fabrication errors of the DPW technology and have shown that with these accuracies we can build up an assembly chain which includes micro-spheres, to create a reliable photonic package. The most severe inaccuracies which were introduced in our tolerance study occured due to rotational errors of the adhesive bonding of the chip into its package.

In the near future we will continue to push the limits of the Deep Proton Writing and Laser Ablation technology to further explore the different opportunities we believe micro-optical interconnect modules have to offer, in an effort to tackle and alleviate the interconnect hurdles at the printed circuit board and at the intra-MCM level.

ACKNOWLEDGMENTS

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FABRICATION OF FLEXIBLE OPTICAL PRINTED CIRCUIT BOARD (FO-PCB)

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ABSTRACT

We report on the fabrication of a flexible optical interconnection module that has been incorporated as a part of an optical printed circuit board (O-PCB). Optical waveguide arrays are fabricated on flexible polyethylen terephthalate (PET) substrate by UV embossing technology. Electrical layers carrying vertical cavity surface emitted laserdiode (VCSEL) and photodiode (PD) array are attached to the optical layer. We measured optical losses of the flexible waveguide arrays bent over various curvatures and characterized transmission performances of the flexible optical PCB (FO-PCB) module. FO-PCB performed high speed optical interconnection between chips over four waveguide channels up to 7.5Gbps on each.

Key Word: Flexible Optical printed circuit board, optical interconnects, UV embossing method, advanced packaging

1. Introduction

Electrical interconnects in high speed inter-chip interconnecrion over gigabit data transmission are facing many severe problems such as bandwidth limitation, signal sitortion and electro-magnetic Interference (EMI). Many attempts have been made to solve the problems of inherent electrical interconnects.[1-8] Optical interconnects have shown possiblity potentail possiblitiy to overcome the limitations of the electrical interconnects for gigabits data capacity. [1-8] However, optical interconnection has many advantages over electrical interconnection such as high bandwidth, light weight, immunity to EMI, low skew and jitter, no need of ground line, and no need of impedance matching. [3-6]

We fabricated an O-PCB module to carry out 5Gbps inter-chip optical interconnection. We placed special emphasis on three facts for manufacturing of O-PCBs. One approach is fabricating the 45° end-mirror reflectors of a waveguide concurrently at the time of fabricating the polymer waveguide by embossing. This is to reduce the number of processing steps and the fabrication cost. Another approach is to provide flexibility on O-PCB modules. In order to provide flexibility we do not fabricate optical layer on rigid substrate such as glass substrate, but on flexible substrate such as polymeric substrate. The other approach is to simplify the alignment between the VCSEL/PD-array and the waveguide array.

This paper presents a successful demonstration of a prototype FO-PCB. And we were able to measure the transmission speed up to 7.5Gbps. We describe in detail the fabrication process of the FO-PCB.

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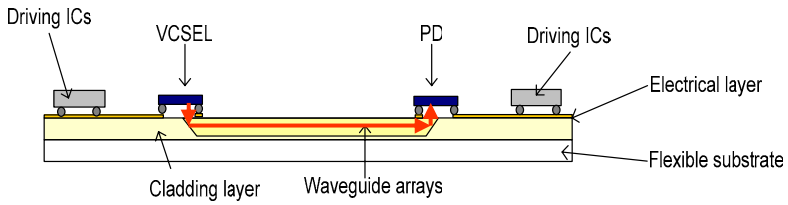


Fig. 1. Conceptual schematic diagram of a FO-PCB module.

2. Fabrication Process

Fabrication of Waveguide Array

To fabricate an O-PCB interconnection module we fabricate polymer waveguide arrays by UV embossing and then form electrical transmission lines to drive the sources and detectors on the waveguide arrays. Fig. 1 shows a scematic diagram of a prototype of an O-PCB module that we fabricated.

We fabricated polymer waveguides for optical layer by UV embossing using silicon mold. Silicon mold is used to form waveguide patterns on flexible substrate. UV curable polymers are used as waveguide materials both the core and the cladding layer.

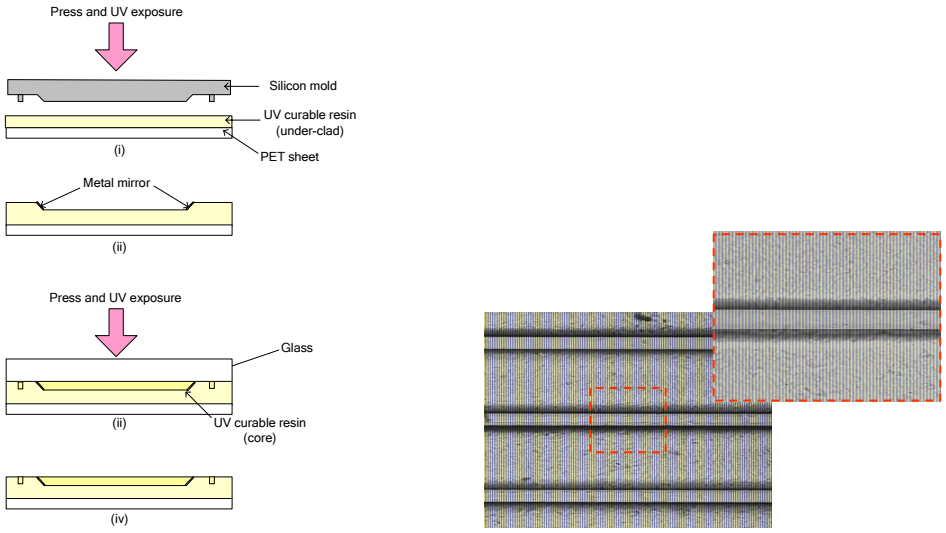
To fabricate a silicon mold we first etched a silicon substrate with wet or dry etching to form a rectangular parallelepiped waveguide arrays. And the end of the silicon mold is wet-etched with KOH-saturated isopropanol solution into a 45° slope. [9] There mirror faces cut at 45-degrees at each end of the waveguide are used for vertical lightwave coupling between the VCSEL/PD array and the waveguide array. The fabricated mold went through a diclorodimethylsilane (DDMS) based self-assembled monolayer (SAM) coating that is used as an anti-sticking layer during embossing process. [10]

Fabrication process of an optical waveguide array is shown in Fig 2(a). First, to prepare the under-cladding and upper-cladding layer, UV-curable polymer with refractive index of 1.45 at 850nm wavelength, is coated on the FET substrate up to 40microns thickness and UV-cured.

The under-cladding layer is imprinted by a silicon mold and is ceased with UV irradiation with 7bar press for 2min. Next, the silicon mold is detached.

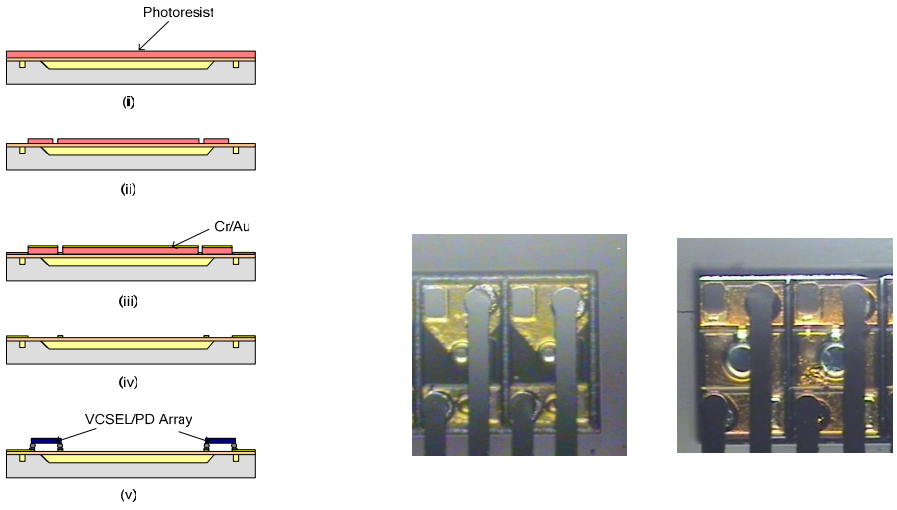
After detaching the mold, a metal thin film is coated on the 45° slope at the ends of the waveguides to enhance the vertical coupling efficiency.

Another UV curable polymer with refractive index of 1.50 at 850nm wavelength to be used for core layer is dropped over the embossed under-cladding layer and is covered with upper-cladding polymer layer. This entire optical layer is pressed at 7bar and is irradiated by UV source. UV-imprinted waveguide array is completed. The cross-sectional dimension of the fabricated waveguide arrays is 50 microns in width, 50micorns in height and 7cm in length. The waveguides are laid out in a pitch of 250 microns to match the size of the fiber.



(a) (b)

Fig. 2. (a) Fabrication process of an optical waveguide array and (b) the optical microscopic view of the fabricated flexible optical waveguide (top view)



(a) (b)

Fig. 3. (a) Fabrication process of the electrical transmission lines and flip-chip bonding and fabricated flexible optical printed circuit board. (b) Bottom views of the VCSEL and PD array after chip bonding

Fabrication of Electrical Layer and Flip-Chip Bonding

Fig. 3 shows the formation processes of an electrical transmission layer to be integrated with the O-PCB optical interconnection module shown in Fig. 1. The electrical metallic layer for transmission line is formed with a lift-off process. On the substrate, a 10micron thick photoresist layer is spin-coated and patterned as shown in Fig. 3(a)-i. At the time of the photoresist patterning we establish the alignment between the optical

layer and the electrical layer using alignment marks which are already placed at the time of fabricating the optical layer. A 100nm Cr/300nm Au layer is sputtered using biased sputter on the patterned photoresist as shown in Fig. 3(a)-iii. These patterns are used as the transmission lines and the alignment marks. After the photoresist is removed, the electrical transmission lines are left on the substrate, as shown Fig 3(a)-iv. The VCSEL and PD array operating at 850nm wavelength are flip-chip bonded on to the substrate, as shown Fig. 3(a)-v. These VCSEL and PD array included solder ball bumper with 80um diameter and 65um height. Fig 3(b) show bottom views of VCSEL and PD array after chip bonding. Bonding accuracy is about 5um.

3. Performance Measurements

Propagation Loss and Bending Loss

In order to evaluate the quality of the optical waveguide array we measured the propagation losses by the cut-back method. We also measured the vertical coupling loss at 45° mirror facet of waveguide array. By the cut-back method the losses of propagation and of the insertion are -0.32dB/cm and -1.91dB/facet, respectively, at butted coupling facet. We coupled the light source into the waveguide vertically via 45° mirror facet and measured the optical power by power meter at the other end of waveguide. We calculated vertical coupling loss at 45° mirror facet as -3.03dB/facet.

We measured the bending losses of the flexible waveguide array as shown Fig. 4. We give bending curvature to flexible waveguide with metal rod shown in the inset of Fig 4. The flexible waveguide yielded no additional loss until around 2 mm radius curvature and above.

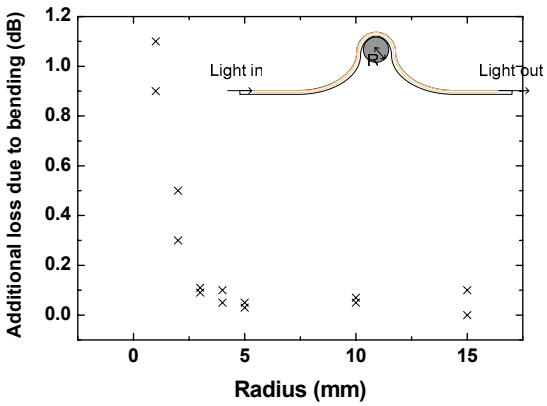
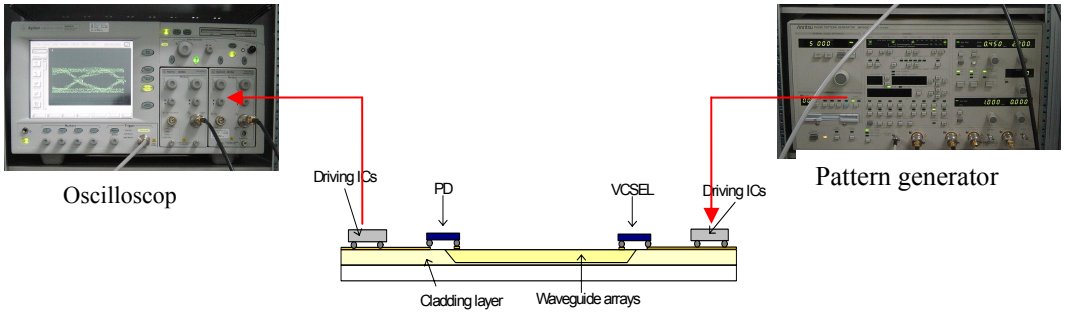


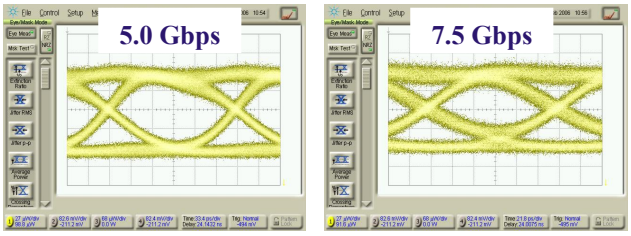
Fig. 4. Bending losses of flexible waveguide array at the various curvatures

Transmission performance

Experimentally, we tested the transmission performance of each waveguide channel up to 5Gbps data stream. A 5Gbps data stream from a pseudo-random binary system (PRBS) was put in to one of the four channels of the O-PCB via VCSEL driver. The VCSEL converts the electrical signal into an optical signal, which then propagates along the waveguide and is converted into electrical signal via a photodetector (PD). The electrical output signal from the PD is then connected to a wide-band oscilloscope and a clear 5 and 7.5Gbps eye pattern was observed.



(a)



(b)

Fig. 5. (a) Experimental setup for evaluation of FO-PCB and (b) the observed 5Gbps and 7.5Gbps eye-diagram.

5. Conclusion

We fabricated a flexible O-PCB using polymer-based flexible waveguide array on polymer-based substrate by UV embossing. For UV embossing we used a silicon mold. For modular form we fabricated an electrical layer carring VCSEL, PD and their driving circuit. And we plased the electrical layer over the optical layer. We measured that F-OPCB has low loss with large bending, respectivley, and perform good optical tranmission up to 7.5Gbps per each channel.

6. Acknowledgement

This work has been supported by the Korea Science and Engineering Foundation (KOSEF) through the Grant for the Photonics Integration Technology Research Center (R11-2003-022) at the Optics and Photonics Elite Research Academy (OPERA), Inha University, Incheon, South Korea.

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Nanophotonic Devices and Systems to Enable Optical Interconnects

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Abstract: Recently a number of successful free-space chip-to-chip and board-to-board optical interconnects have been demonstrated. Here we present some of the results that can be derived as a result of this work.

I. INTRODUCTION

Parallel optical interconnects are capable of providing high bandwidth communication links both within and between high performance electronic systems. The advantages of optical communications for long-distance interconnects are well known, and provide the motivation for modern optical fiber networks. Optics is now challenging copper at shorter and shorter distances. The benefits of optical interconnects include reduced signal distortion and attenuation, lower power requirements, lighter components, potentially lower costs and much greater immunity to electromagnetic interference. A thorough review of these physical issues is provided in references [1, 2]. In the commercial arena, several manufacturers now supply optical fiber ribbon-based parallel optical data links (PODLs) of 8 to 12 channels, operating at data rates of up to 3.25 Gb/s per channel over distances of 100-1000 m (depending on bit rate). However, there are applications where many more parallel channels are required and in some cases the interconnect configuration is more complex than a simple point-to-point link. For example multiprocessor computers, telecommunications switches and embedded systems all require highly parallel interconnections. In particular the concept of the direct sourcing and termination of optical signals on silicon has been proposed as a method to relieve the off-chip communication bottleneck. Figure 1 is a schematic representation of this concept. In recent years significant progress has been made in the enabling technologies for parallel optical interconnects for digital systems. This includes the hybrid integration of Vertical Cavity

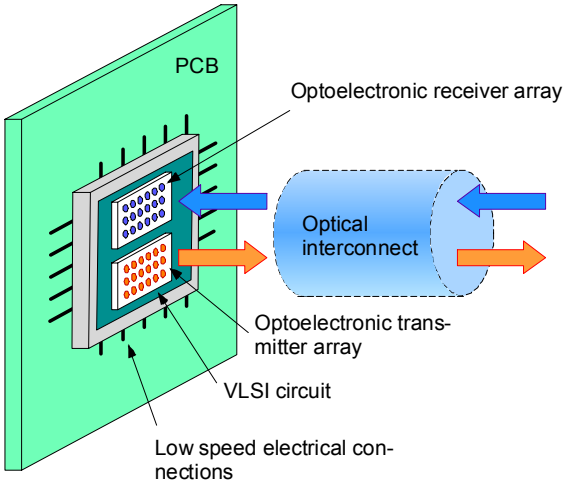

Figure 1: Schematic representation of a board-to-board parallel optical link with direct termination of optical signals on chip.

Cavity Surface Emitting Lasers (VCSELs) and photodiodes with silicon integrated circuits (also referred to as optoelectronic VLSI or OE-VLSI), assembly techniques for Free-Space Optical Interconnects (FSOIs), the development of fiber

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arrays and the integration of optical waveguides with printed circuit boards.

In this paper we refer to a set of design rules afor free-space optical interconnects for chip-to-chip and board-to-board communication. These rules have emerged after implementing a series of optical interconnect demonstrator systems and subsystems, including a 512 channel optical ring interconnect [3, 4], a 512 channel bi-directional interconnect [5, 6], a 1080 element OE-VLSI chip which implements a variety of data transmission protocols [7, 8] and a highly misalignment tolerant interconnect that makes use of spatial redundancy [9]. Through the realization of these systems, we researched a range of areas, including optoelectronic devices, electronic circuit design and, optical design and packaging.

In developing both rules and systems, we made several assumptions: (1) we assumed that the optical source in a free-space optical interconnect was a VCSEL, and may be either single mode or multimode; (2) we assumed heterogeneous integration using flip-chip bonding and substrate removal of optoelectronic devices with ASIC based transceiver and processing logic (reviewed in detail below); (3) the optoelectronic detectors were GaAs p-I-n diodes.; (4) the optical interconnect distance was less than 150 mm (i.e. characteristic of inter-chip and board-to-board spacings); (5) the interconnects were rigid free-space optical systems; (6) the interconnect was a point-to-point transmissive topology; (7) the interconnect incorporated a realistic tolerance to misalignment. Our research has been based on the use of GaAs optoelectronic devices and so the wavelength of operation is 850 nm. However, many of the guidelines can be adapted to other wavelengths.

II. Design Space

Through the realization of demonstration systems, we identified the design space in which chip-to-chip and board-to-board communication using optics was valid. Since the technology is aimed at future high performance electronic systems, we refer to the International Technology Road Map for semiconductors [10]. Figure 2 shows the projected increase in VLSI transistor on-chip clock speed, off-chip clock speed, number of high speed off-chip clock lines and total off-chip I/O capacity as a function of time for high performance systems, taken from reference [10]. It can be seen that by 2014 the off-chip clock speed is projected to reach 1.8 GHz and the width of the off-chip bus is also projected to increase to 3000 high speed lines, with a total projected off-chip I/O capacity of 5 Tb/s. The on-chip clock speed is projected to reach 13.5 Gb/s. From this data we obtained a view of the design space for off-chip interconnects by the year 2014, under the assumption that the necessary off-chip bandwidth will be 5 Tb/s. This is shown in Figure 3, where the data rate per channel necessary to achieve 5 Tb/s is plotted as a function of the number of parallel channels. We have shaded different regions corresponding to different optical interconnect formats. As is indicated in Figure 3, fiber ribbons (1-D structures with 12 to 32 fibers) are well suited for interconnects required modest parallelism and high data rates. Fiber array based interconnects are well suited for channel counts of order 10's to 100's operating at high data rates as well.

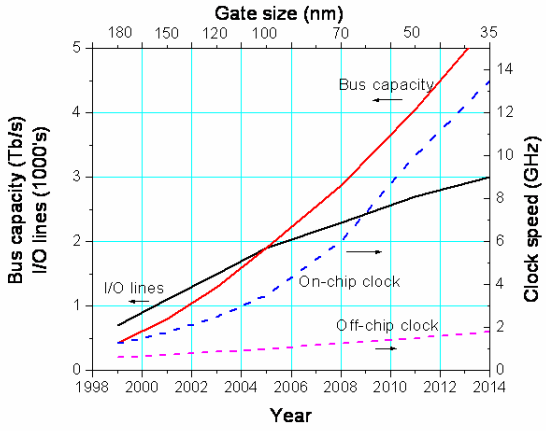


Figure 2: Projected evolution of on-chip clock speed (dashed line, right axis), off-chip clock speed (dotted line, right axis), number of high speed I/O lines (dash-dot line, left axis) and total bus capacity (solid line, left axis) as a function of time and transistor size for high performance systems.

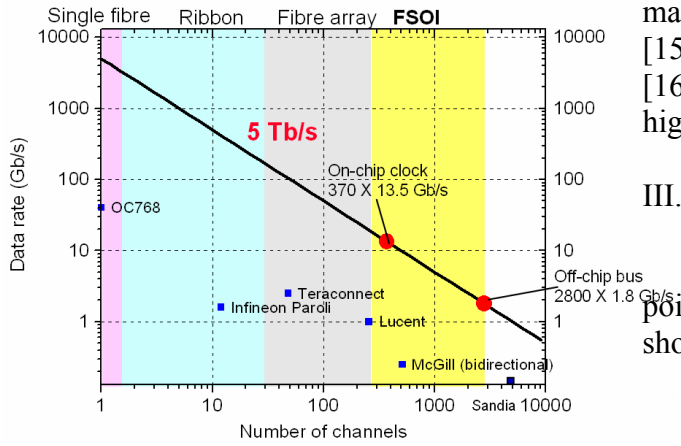


Figure 3: Projected off-chip I/O requirements for 2014.

At present fiber arrays of 8 x 8 to 16 x 16 have been demonstrated [11, 12] but volume fabrication of these elements remains to be properly developed. Even a 256 channel fiber array would require per channel data rates of 19 Gb/s. Moreover, for the very short distances that we consider here, the limited bending radius and high fabrication cost of fiber arrays may render them impractical. From Figure 3 it is apparent that if we assume that the optical interconnect channel data rate is not to exceed the projected on-chip data rate of 13.5 Gb/s (which would otherwise require the use serialization/deserialization circuits) then a 5 Tb/s aggregate data rate implies the presence of 370 optical lines. If we assume that the off-chip optical links run at the projected electrical off-chip clock speed of 1.8 Gb/s then this implies approximately 2700 optical lines. We suggest that these two values represent the boundaries for optical solutions to the off-chip interconnect problem, and that they also represent the domain in which FSOI's represents a possible solution. Several experimental free-space interconnects have achieved the lower end of the parallelism range [13, 4, 6, 14] and we have recently reported an OE-VLSI ASIC with 1080 optical I/O that approaches the middle of the required parallelism range [7, 8]. Other researchers have demonstrated matrix addressed VCSEL arrays with 4096 outputs [15]. Fiber image guides and fiber image conduits [16, 17, 18] represent another possible alternative high density interconnection medium.

III. A Representative FSOI

An example of an experimentally realized point-to-point free-space optical interconnect is shown in Figure 4.

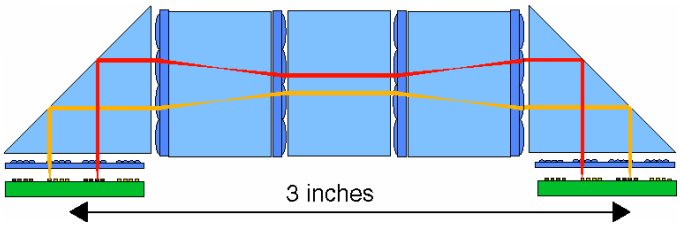


Figure 4: Generic free-space optical interconnect.

In this system two OE-VLSI chips were bi-directionally interconnected over a distance of 3 inches. Each chip contains 256 transmitters

(VCSELs) and 256 photodetectors and operates at a wavelength of 850 nm. The interconnection distance was selected such that by inserting two additional prisms into the beam path it could interconnect two boards in a bookshelf configuration. The relay optics was based on clustered diffractive lens and the array density that was achieved was 28 channels/mm^2. A photograph of this system is shown in Figure 5. This system illustrates the necessary components of an optical interconnect, including the ASICs to be interconnected, a PCB (or MCM substrate) on which the ASICs reside, the optical system used for interconnection, and the optical packaging required to realize the link.

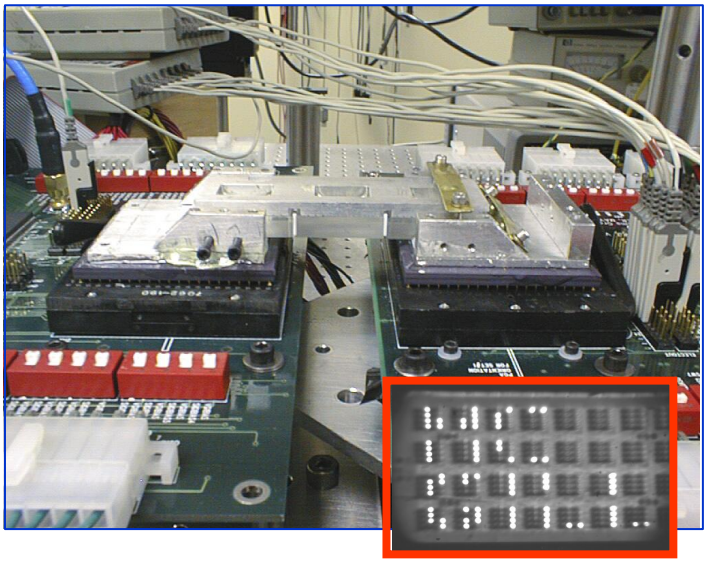


Figure 5: Photograph of an experimentally realized 512 channel inter-chip interconnect system.

In designing a system, some of the issues which must be addressed are: ASIC type, transceiver architecture, digital functionality, optoelectronic devices used in the interconnect, relay optics and the various packaging levels, including electrical packaging (which concerns issues such as signal integrity and power dissipation), optoelectronic packaging (which concerns the attachment of the optical components to the OE-VLSI chip) and the optical packaging (which concerns the assembly of the relay optics). Finally it is necessary to consider the way that these different aspects interact with each other.

A key enabler in this technology is the intimate integration of optoelectronic devices with an ASIC substrate. In the following section we describe methods used for realizing the Optoelectronic-VLSI chips and associated packaging used in our system demonstrators. By example, we articulate appropriate design guidelines we have employed while constructing these devices.

III. OE-VLSI Chip Design

This section is organized as follows: in Section A we describe heterogeneous integration techniques we have used, and in Section B we describe the two transceiver architectures and comment on the suitability for each. We also discuss the functionality we have embedded into our OE-VLSI circuits to enhance signal processing capability. Our approach in designing these OE-VLSI ASICs is consistent with the philosophy that the optics are used for interconnectin and the electronics are used for transceiver functions and DSP.

A. Heterogeneous Integration

We used heterogeneous integration to achieve the high density optical I/O. In doing so, it was important to assure compatibility of ASIC metals with the metals used in the flip-chip bump bonding. A related issue is the need to insure alignment of ASIC connection points with III-V device contact points. In the following sections we summarize our flip-chip bump bonding based heterogeneous integration strategy. To achieve the OE-VLSI ASICs described, 2-D arrays of VCSELs and PDs were fabricated on separate substrates and subsequently integrated onto the ASIC die. In order to support a compact high-density micro-

optical interconnects described above, the VCSELs and PDs were interleaved. We describe in this section: the design and target operating properties of the VCSELs and PDs, the OE device layout geometries, and heterogeneous integration techniques including flip-chip bonding and substrate removal of the interdigitated OE devices.

1) VCSEL and PD Design and Specifications: The VCSELs used in our designs were designed to operate at 850 nm with threshold currents of 1.0 to 4.5 mA and slope efficiencies of 0.25 to 0.35 mWs/mAs. The devices were also designed to be backside-emitting because of the desire to flip-chip bond them to ASIC driver circuits as described below. This necessitated removal of the GaAs substrate to minimize absorption of light. To achieve these objectives, VCSELs were fabricated with both the n-contact and the p-contact located on the top surface of the wafer to facilitate electrical contact to the ASIC circuits. Figure 6 shows a schematic of the VCSEL geometry indicating emission direction after substrate removal and integration to the ASIC. The p-contact was formed above the top distributed Bragg mirror (DBR) and the n-contact was brought to the substrate surface through mesa isolation and ion implantation. Figure 7 is a photomicrograph of four isolated VCSELs prior to flip-chip bonding and substrate removal. The VCSELs in the photograph are on a 125μm x 125 μm pitch. Once bonded to the ASIC as per the description give below, the n-contact and the DBR became the top (emitting) surface of the VCSEL. The photodiodes were P-I-N structures designed to operate with a responsivity of 0.5 mA/mW. The 2-D arrays were fabricated at the wafer level on a 125 μm x 125 μm pitch with p and n contacts brought to the surface.

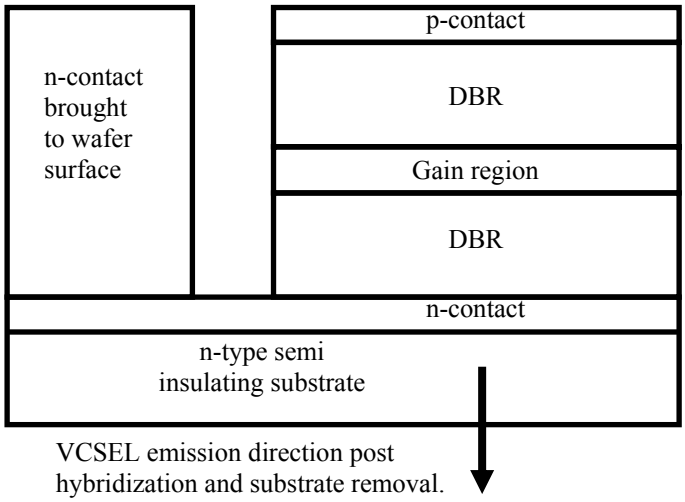


Figure 6: Schematic of the VCSEL geometry indicating the emission direction post substrate removal.

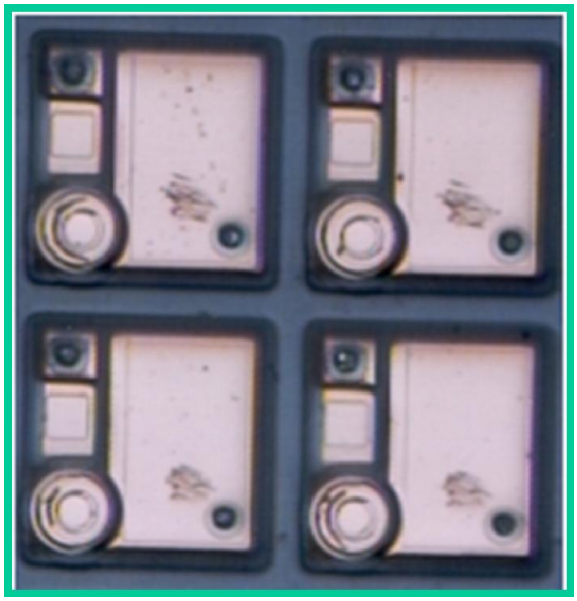


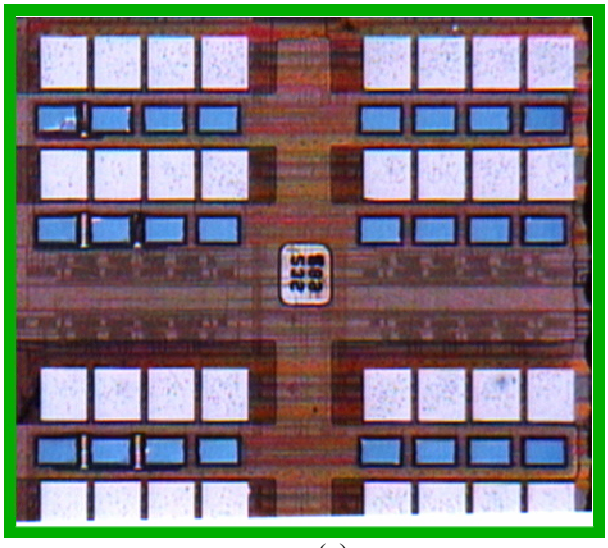
Figure 7: Photomicrograph of four isolated VCSELs prior to flip-chip bump bonding.

2) Optoelectronic Device Layout Geometry: In order to support a compact point-to-point optical interconnect system, as shown in Figure 4 and Figure 5, the VCSELs and PDs were interleaved and arranged in a clustered geometry. VCSELs and PDs were grouped together in clusters, and within

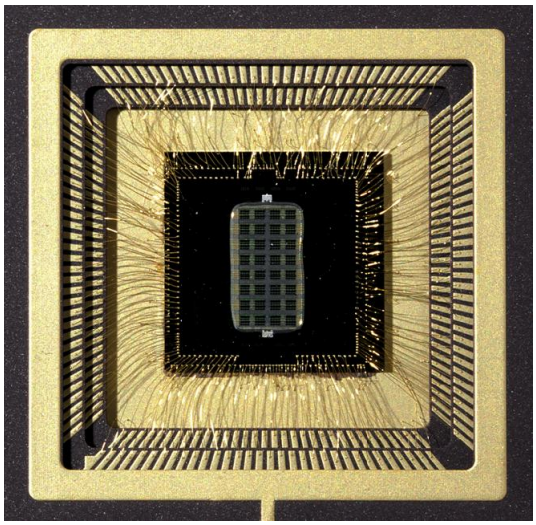
each cluster, rows of VCSELs and PDs were interleaved. Specifically, a cluster consisted of eight VCSELs and eight PDs arranged in four rows. The pitch of the optoelectronic devices was 125 μm in both the horizontal and vertical directions; therefore, the VCSELs and PDs were on 125-μm horizontal by 250-μm vertical pitch. The complete 256-VCSEL and 256-PD array consisted of 32 clusters arranged in eight rows and four columns. The center-to-center spacing of clusters was 750 μm horizontally and 750 μm vertically. The driver ASIC was designed to accommodate this OE device pitch and placement.

3) Heterogeneous Integration and Substrate Removal: The VCSELs and PDs were integrated onto the CMOS driver using flip-chip bonding and substrate removal techniques. The VCSEL flip-chip contact area was 15 μm x 15 μm and the PD flip-chip contact area was 10 μm x 10 μm. The contact areas on the CMOS die for the VCSEL driver and PD receiver were identical to those on the optoelectronic devices. Heterogeneous integration was accomplished by employing relatively conventional photolithographic processes to deposit and lift off contact metals and the wafers followed by a precision assembly process using a flip-chip bonding tool. In the photolithographic step, a photoresist polymer was first spun out on the wafer and printed with the contact metal pattern and then developed. Indium was then evaporated onto the wafer and the photoresist was lifted off, leaving metal on the contact pads. This process was used for the VCSEL and PD wafers and the CMOS dies. The individual OE device dies were separated by mechanical dicing and then integrated onto a CMOS die using the precision alignment hybridization tool. The VCSEL die was first attached to the CMOS chip followed by dry etching to remove the substrate; integration of the PD die was accomplished next followed by substrate removal. The bonding of the indium metal contacts on the CMOS chip and on the OE devices was accomplished through a combination of force and controlled temperature. The process resulted in electrical isolation of individual OE devices and allowed the interleaving of the VCSEL and PD devices onto a single CMOS die. Although individual dies were used to assemble this generation of OE-VLSI chips, migration of the process to the wafer level is relatively straightforward.

Figure 8a shows a photomicrograph of four clusters after heterogeneous integration and substrate removal, each cluster consisting of eight VCSELs and eight PDs hybridized to the underlying CMOS chip. Figure 8b is a photograph of the complete OE-VLSI chip after VCSEL and PD integratation. Using continuous wave measurements, the VCSEL yield after heterogeneous integration was >98%.



(a)



(b)

Figure 8: a) Four clusters after heterogeneous integration; b) Complete OE-VLSI ASIC chip.

We have found the above process to be very effective in realizing the OE-VLSI ASICS used in our systems to date. As suggested, the process is relatively straightforward and can be extended to wafer level integration of devices with wafers of optoelectronic devices. The process lends itself to high levels of integration thus permitting large optical I/O counts.

4) Transceiver Architectures: There are numerous possibilities with respect to transceiver design for OE-VLSI technology. We have employed both single ended and differential designs. In the following section, we describe the two topologies including the merits of each.

In [5], the main objective of the transceiver circuit design was to provide enough flexibility to allow for the successful simultaneous operation of large numbers of transmitters and receivers. It was expected that the VCSEL, and PD characteristics would vary over a large device array; thus, the transceiver designs had to allow for statistical variations in device parameters and had to avoid dependence on parameters specific to the silicon and the OE process. The transceiver circuits were designed to keep their inherent switching noise generation at a practical minimum, as well as to be immune to the expected presence of the substantial amounts of aggregate switching noise generated from a large array of missed analog and digital circuits.

Given these design objectives, the design of the laser driver was based on current-steering. Specifically, a VCSEL was dc-biased with a current IBIAS to a point above the VCSEL threshold current. Modulation current was provided by the current source IMOD and was steered through either the VCSEL or through an electrical dummy diode load, which was implemented as a diode-connected PMOS transistor power. The current-steering nature of the laser driver allowed the total current drawn from the power supply to remain nominally constant at IBIAS + IMOD whether the VCSEL was in a high or low output power state. Power supply current transients could not be completely eliminated due to the mismatch in electrical parameters of the dummy load D1 and the VCSEL, but the approach allowed current transients (*dI/dt* noise) to be kept to a small fraction of the IMOD. The range of currents settable for IMOD AND IBIAS was approximately 6 and 12 mA, respectively.

The receiver circuits used in [5] were optically and electrically single-ended and were based on a common source transimpedance amplifier (TIA) front end. An offset-control stage was included to compensate for both the dc-coupled nature of working with amplifier stages and the de-coupled nature of the optical input. This allowed properties of the receiver such as sensitivity (preamplifier feedback resistance) and the accommodation of various average optical power levels (offset control) to be dealt with independently, providing greater operational flexibility. The final stage of the receiver consisted of a Schmitt trigger that served as a final gain stage

for decision-making and provided some hysteresis in its transfer function to help reduce the effects of power-supply switching noise in an array environment. Via the heterogeneous process described above, each driver circuit was integrated with a VCSEL and each receiver was integrated with a PD; this resulted in a 2-D array of 256 transmitters and receivers.

In addition to the above, chip, we have designed, fabricated, and tested an OE-VLSI ASIC that employed a fully optically and electrically differential architecture. The details of this chip are presented in [7, 8] and will only be summarized here. Transmitters and receivers were implemented as fully differential circuits, both optically and electrically. Using optically differential signaling allowed the receiver to determine a decision threshold based on the optical input signals on a per-receiver basis. A fully differential electrical architecture allowed for reduced switching noise generation on the power supplies and enhanced rejection of common-mode noise. The transmitters and receivers were designed for operation at a data rate of 250 Mb/s. Additional circuit elements were added to the transmitter and receiver circuits to allow for circuit testability prior to OED integration. These circuit elements were placed in parallel with the normal locations of OEDs, and could be specifically enabled by test inputs. To further enhance testability and operability, configurable parameters such as the magnitude of the modulation and bias current magnitudes and the magnitude of the feedback resistance the receivers could be set using digital inputs.

V. Conclusions

Through the design, fabrication, and testing of these two large-scale OE-VLSI ASICs and numerous test chips in which different receiver and transmitter topologies were employed, we draw upon analytical, experimental, and simulation-based work to arrive at a number of core conclusions. Firstly, there needs to be some method of controlling the key set point parameters of the laser drivers and receivers across a sub-set of the entire array. This leads to higher operational yield. Secondly, the use of an optically and electrically differential architecture for the receiver and transmitter designs is optimal for OE-VLSI applications. Through our work, we have found that an optically and electrically differential architectures facilitate or optimizes the implementation of several critical aspects of OE-VLSI ASIC design, including: 1) Design for testability concepts and implementation for receiver and transmitter circuits; 2) the receiver and transmitter circuit generation of, and immunity to, switching noise on the voltage supply and ground rails and through the substrate; 3) the improvement of operational yield (percentage of functional circuits in a group of circuits that meet bit-error and data rate targets) in common bias and control receiver groups; and 4) the reduction of intra-channel receiver skew in parallel digital synchronous OE-VLSI applications and the reduction of individual receiver latency.

VI. Acknowledgements

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VII. References

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Application of two-photon 3D lithography for the fabrication of embedded ORMOCER® waveguides

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ABSTRACT

The idea of applying the two-photon 3D lithography (2P-3DL) to an industrial printed wiring board (PWB) fabrication process is quite pioneering. Taking advantage of the unique rapid prototyping properties of 2P-3DL - its particularly inherent true 3D capability and its high flexibility in processing- this lithographic method can be adapted and optimized concerning the direct laser-writing of integrated optical interconnects with tens of microns in diameter. This will push the method forward towards industrial fabrication of next generation PWBs with integrated optical layers, and put it on the leading edge of printed circuit board (PCB) technology.

In this context, the concept of a direct laser-written embedded waveguide is based on the local increase of the refractive index of the exposed material, which is triggered by two-photon absorption (TPA) at the laser focus. The laser induced refractive index difference forms the core of the waveguide, whereas the unexposed surrounding material forms the cladding. Thus, only one optical material is required to form the waveguide using true 3D lithographic process compared to other devices, which significantly simplifies processes. The material is subject to stringent requirements concerning the PWB production process: beside its high refractive index change, a low optical loss of the fabricated optical interconnect is required. The integration of the waveguide into the volume of the material also requires thick films up to 500 µm on the PWB substrate, and the material has to withstand the complete PWB fabrication process, where the board is chemically treated and exposed to high temperatures as well as high pressure during the lamination processes of subsequent metal layers.

For this application, an inorganic-organic hybrid polymer (ORMOCER®) film is applied, casted onto a PWB substrate, and the two-photon 3D lithography system parameters and optics are tuned such that waveguides with a diameter of approx. 30 µm can be inscribed. The board is equipped with laser- and photodiodes, which are totally covered by the thick ORMOCER® film. The integration of the waveguide in such a preconfigured board requires precise 3D registration of the sample prior to the waveguide writing in order to align the waveguide relative to the optoelectronic components. By means of the 3D registration, the waveguide alignment is an inherent part of the fabrication process. The 3D capabilities of the 2P-3DL permit not only the fabrication of single embedded waveguides with a simple geometry, but also more complex waveguide structure (e.g. bundles) with largely arbitrary waveguide configurations.

In this paper, we present the development and realization of the two-photon 3D lithography for the fabrication of integrated optical interconnects on PWBs. The ultimate goal of this approach is the large-scale fabrication of leading-edge PWBs with an integrated optical layer for additional functionality. The functioning of the fabricated and embedded waveguides is demonstrated by measurements of the essential parameters of such an optoelectronic system (photocurrent, optical loss, throughput, etc).

Keywords: two-photon 3D lithography, inorganic-organic hybrid polymer, ORMOCER®, waveguide, integrated optical interconnect

1. INTRODUCTION

Laser-based micro-machining is pushed to new dimensions by the advent of stable and reliable femtosecond laser sources. Due to the high peak power of ultrafast laser pulses, femtosecond lasers are able to process virtually any material. The fast deposition of the moderate laser pulse energy in the target material on a femtosecond time scale leads to better quality of micro-machining features than lasers applying nanosecond pulses. Femtosecond lasers are not only used for a superior surface processing based on laser ablation, but also for high-resolution three-dimensional patterning

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of transparent media, where the laser-matter interaction relies on non-linear absorption. A non-linear laser-matter interaction such as the two-photon 3D lithography based on the simultaneous absorption of two photons from a laser pulse exhibits certain features that can be exploited for advanced micro-fabrication: the energy transfer from the laser to the material remains strongly localized around the laser focus. This aspect together with the transparency of the target material for the laser wavelength due to the absence of linear absorption enables true 3D direct laser writing of complex structures into the volume of a material. Since the patterning takes place inside the material, there is no special requirement for vacuum or inert gas atmosphere during sample processing as well as for complicated processes as for standard stereolithography. The spatially limited interaction between the laser and the bulk material modifies chemical and/or physical properties of the target material, for example the solubility, or the refractive index. This effect is utilized for the fabrication of 3D micro-devices and building blocks for M(N)EMS/M(N)OEMS, and other photonic micro- and nano-systems. Femtosecond lasers have been used in the field of photonics for waveguide fabrication in glass [1, 2], complex three-dimensional structures employing two-photon microstereolithography in organic-inorganic hybrid materials [3], photonic crystals [3,4,5], and many more. A very detailed and comprehensive survey over the development is found in [6].

The application of two-photon 3D lithography for the fabrication of embedded waveguides on PWBs is motivated by the increasing demand for higher data rates that puts optical information paths as an alternative to high frequency electrical information paths on PWBs into the focus of research. Key issues in this topic are adequate polymer materials with low optical losses, waveguide fabrication concepts (structuring methods), coupling concepts, and process compatibility (lamination). Fabrication concepts of optical core layers in PWBs usually use two different polymer materials with different refractive indices for the core and the cladding layer, respectively, where the layers are usually built up sequentially. Embedded waveguides are photo-lithographically patterned and buried in the cladding material [7]. This approach requires sophisticated coupling methods between waveguides and electro-optical components on the board. Inadequate coupling increases optical losses drastically, and leads to higher bit errors and reduced communication bandwidth.

In this paper, the adaptation of the two-photon 3D lithography for the fabrication of an integrated waveguide system with an inorganic-organic hybrid photosensitive material (ORMOCER®) is presented as a novel approach. Provided that a suitable material is available, the need for separate cladding and core materials becomes redundant, and the coupling between waveguides and electro-optical components on the board becomes an intrinsic part of the patterning process. The latter leads to a significant cost reduction for processing and integration.

2. MATERIAL AND METHODS

ORMOCER®, a sol-gel based material, has already proved to be suitable for a two-photon based micro- and nanofabrication for photonic applications [8]. In the case of an inorganic-organic photosensitive hybrid material, the two-photon absorption induces a localized photo polymerization via a photo initiator, where the material acts as a negative type photoresist. The photopolymerization locally increases the refractive index upon laser irradiation in the focal volume, thus forming the core of an embedded waveguide without the need for a further development of the unexposed material which acts as a cladding. This simple method enables also the in situ coupling of laser-written waveguides to optoelectronic components as an intrinsic part of the patterning process.

1. Experimental setup

An amplified ultrafast Ti:Sapphire laser system from Spectra Physics (Maitai - Spitfire combination) is used for the direct writing of embedded waveguides. The laser system provides NIR pulses at 800nm wavelength with a pulse duration of approx. 130fs, and operates at a repetition rate of 1 kHz. A maximum pulse energy of approx. 1mJ can be achieved. The laser pulses are guided through an electro-optical switch that works also as laser attenuator by remote control of the crystal high voltage of the Pockels cell. For improving fundamental spatial Gaussian beam distribution, the laser is subsequently focused through a spatial filter before being guided to the sample and additional diagnostic tools, such as a Femtos single shot autocorrelator and a Spiricon laser beam analyzer (Fig. 1). A He-Ne laser is collinearly guided to the sample, and the back-reflected light of the He-Ne laser is detected by a photodiode in a confocal setup. This feature of the setup permits the measurement of the sample's surface position, and hence a surface mapping of the sample along the waveguide path. A CCD camera which is placed next to the microscope objective, is used for lateral gauging of laser and photodiodes that are attached to the sample PWB, and need to be connected by a laser-written waveguide. The handling of large-area samples with the photosensitive material exposed to ambient atmosphere requires a yellow light environment for the entire system. The laser is astigmatically focused by a 1:3

cylindrical telescope and a 20x microscope objective. The cylindrical telescope reduces the laser beam diameter in one dimension, and allows additional and symmetric shaping of the waveguide's cross-section, which was successfully shown for multi-photon absorption based waveguide fabrication in an Er:Yb doped glass [9].

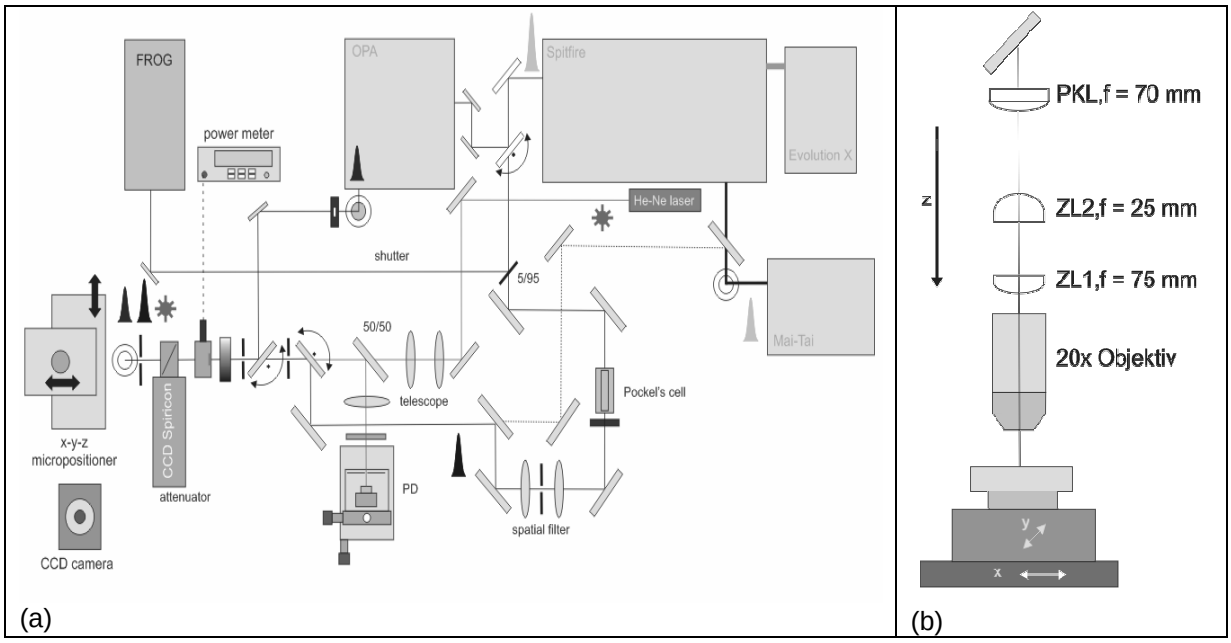

Fig. 1: (a) Scheme of optical setup. Main components of the system are the Ti:Sapphire laser source, the electro-optical pulse picker / attenuator, spatial filter, confocal z gauging setup with photo diode, 3-axes stage, and machine vision. (b) Focusing optics: a 1:3 cylindrical telescope for beam shaping and a 20x microscope objective in a transverse scanning geometry.

2. Inorganic-organic hybrid materials (ORMOCER®s)

Sol-gel-based processing is used to synthesize the ORMOCER® used for 3D waveguide patterning. The material has to fulfill many different requirements, among which the ability of being patternable with the femtosecond laser, a high index step between the exposed and the non-exposed material, a low absorption coefficient, the capability to form thick layers, and the resistance to chemical processing in the PWB process are the most prominent.

The chemical processing typically consists of two steps. In the first step, an Si-O-Si network is established via hydrolysis/(poly)condensation reactions of alkoxysilanes which yields organically modified nanoscaled inorganic-oxidic units, resulting in a prepolymer sol. The sizes of these units usually range from about 1 to 10 nm, dependent on the material system synthesized. In the second step, an organic cross-linking is performed either photochemically and/or thermally, resulting in (patterned) ORMOCER® layers. (Oligo-) methacryl, acryl, styryl, or epoxy groups are often used in order to account for the organic cross-linking, and the resulting material thus behaves as a negative resist.

The material's properties can be chemically tuned by the synthesis conditions, for example by variation of the catalysts, temperature, and alkoxysilane scaffold. This allows one to create tailored materials as required by the application. An overview about applications of inorganic-organic hybrid materials is given in Refs. [10, 11]. In Fig. 2, a schematic sketch of the multifunctional precursors for the hybrid polymer synthesis as well as a brief overview about the variation of material properties is shown.

While for other ORMOCER® materials applied as waveguide materials 3-methacryloxypropyltrimethoxysilane is a commonly used alkoxysilane in synthesis [12], for the material used within this work acrylate-alkoxysilanes with more than one acrylate moiety are employed. This accounts for an increase in the photochemical reactivity, and provides more chemical bonds which then also can result in two- and three-dimensional structural units. The refractive index of this resin is determined by Abbé refractometry (587 nm) to be 1.491 ± 0.002, and its viscosity is around 4.5 Pa·s which strongly depends on the reaction conditions and the variation in the composition of the material. The resin is highly

transparent at 850 and 1310 nm, where the resin's optical absorption was determined by UV-VIS-NIR spectroscopy to be about 0.02 and 0.28 dB/cm, respectively. Besides, the resulting layers can be as thick as several hundred µm with a high aspect ratio, thus making the use of this ORMOCER® feasible for the presented application. One reason for the thick layer capability is its high organic content compared to other ORMOCER® systems. Another reason is given by the good mechanical behavior of the material. Although its organic content is very high, the material can withstand the PWB processing at temperatures as high as 200 °C under a pressure of about 20 bar [13].

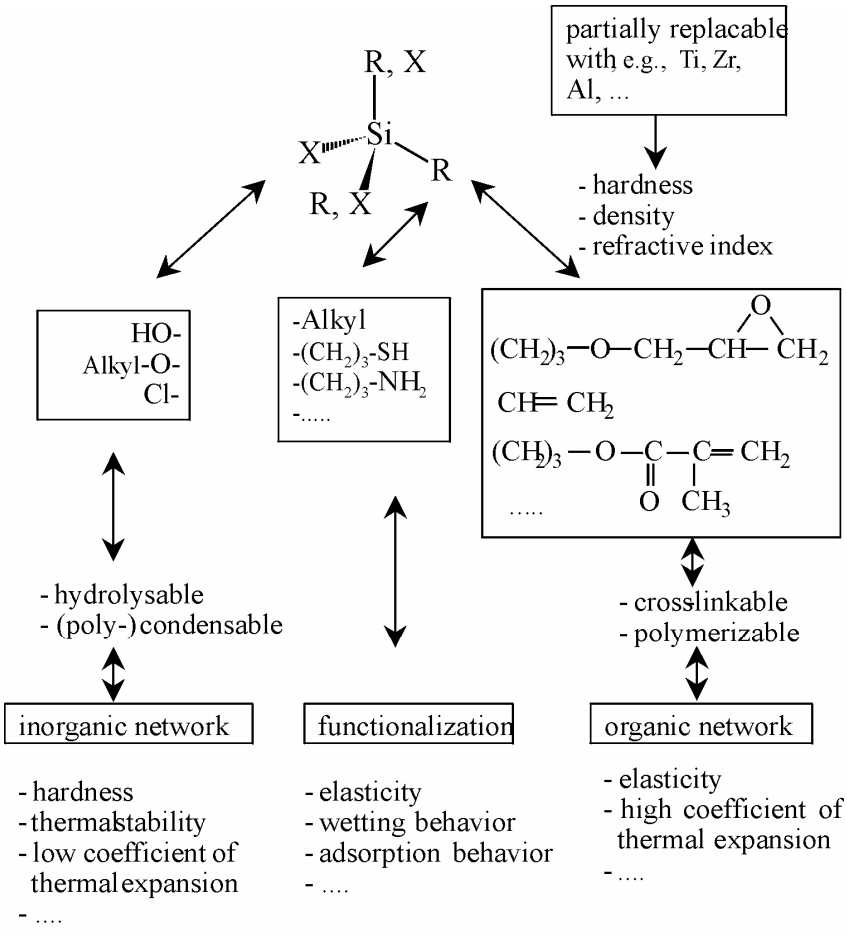

Fig. 2: Schematic sketch of multifunctional precursors for hybrid polymers and the variation of properties.

3. Fabrication of embedded optical interconnects on PWBs

3.1. Material tests

Before the waveguide can be fabricated, material tests are performed in order to derive optimized parameters for the waveguide in terms of laser power, sample feed rate, and alignment of the cylindrical telescope for a nearly circular waveguide cross-section. For this purposes, pieces of a scored board are examined after preparation of the ORMOCER® film and laser writing of simple lines, respectively. Subsequently, cross-sections of these pieces are investigated by optical microscopy, where the depth and the cross-section of the individual waveguides are characterized. At appropriate laser parameters, nearly circular and transparent waveguides are found in the optical film. The same material tests were performed for verification of the waveguide bundle geometry (Fig. 3).

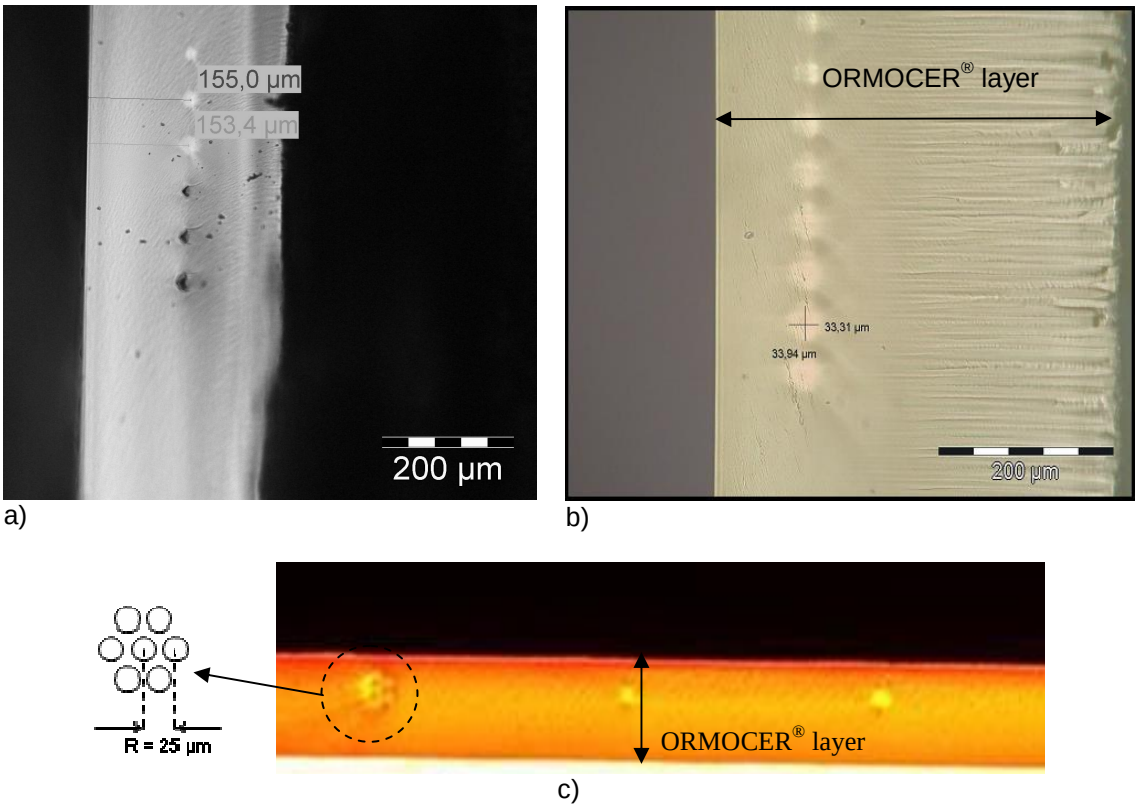

Fig. 3: (a) Material test with ORMOCER®. The laser power is 260, 240, 220, 200, 180, and 160µW (bottom to top), respectively. The depth of the waveguides in the ORMOCER® layer is set to 150 µm. The diameter of the waveguides is approx. 30 µm. Sample feed rate is 20 mm/min. (b) Optical transmission microscopy of a set of straight-line waveguides embedded in an approx. 400 µm thick ORMOCER® layer. The diameter of the waveguides is usually in the range 30-40 µm. (c) Cross-section of the ORMOCER® film on a PWB with inscribed waveguides and a waveguide bundle, as observed by transmission optical microscopy. A sketch of the waveguide and bundle (marked by a dotted circle), which consists of a central line with 6 satellite lines around, is also shown.

3.2. Preconfigured Boards

The used boards for the demonstration of a working embedded optical interconnect between a laser- and a photodiode are either 5 cm or 15 cm long. These boards are provided by our project partner AT&S, the market leader in Europe of printed circuit board production. AT&S is developing innovative approaches to integrate an optical interconnection path (E/O-converter– optical waveguide – O/E-converter) completely into a multilayer printed circuit board. The demonstration boards are equipped with 850 nm VCSELs that are mounted upright on the die edge such that the emitting area of the VCSEL points towards a photodiode. A frame is attached to the boards, which enables the casting of thick ORMOCER® films on the board since a total embedding of the laser and photodiodes is required, and to avoid material flow through the drill holes which are used for electrical connections. The embedding film has to be thick enough to have a planar surface even above the diodes. Any distortions in the optical film may cause problems to the laser writing of the waveguides. Since the laser is focused through the surface, the surface has to have properties that are comparable to an optically flat and smooth surface. The final film thickness was set to be in the range between 300 and 500 µm.

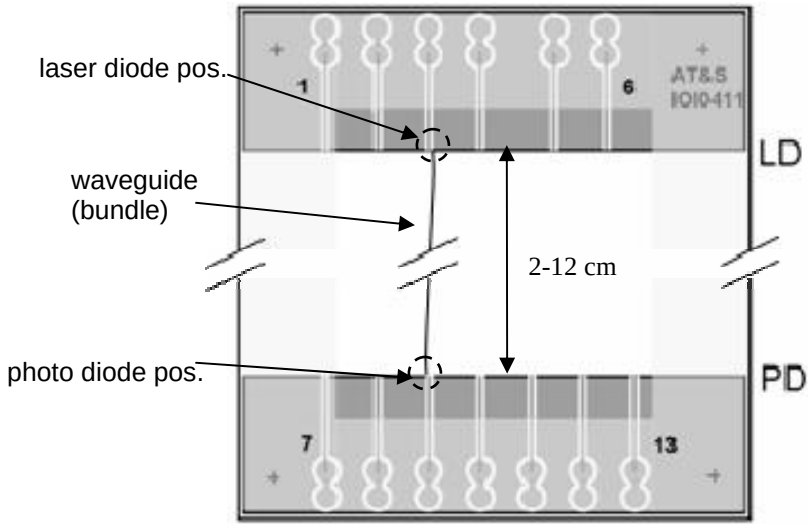

Fig. 4: Layout of PWB samples with integrated optical interconnects. The length of the board is either 5 cm or 15 cm. The length of the waveguides is accordingly either 2 cm or 12 cm. At the side of the LD contacts, a laser diode was placed close to the contact edge. At the PD side, a photo diode was mounted on the opposite contact. The sine-shaped bent waveguides connects the laser diode and the photo diode.

3.3. Two-photon 3D lithography of embedded waveguides

The sample preparation comprises a rough cleaning of the board with lens cleaning paper, a rinse in 2-propanol, and subsequent drying. The ORMOCER® is drop casted on the board and soft-baked on a hotplate at approx. 100°C for 2-5 minutes. The elevated temperature reduces the viscosity of the material, and therefore supports the formation of a uniform thick film on the board. After thermal treatment of the sample, a UV flood exposure under Ar atmosphere is performed. This pre-curing of the ORMOCER® stabilizes the material mechanically. For this purpose, a low power sunlamp is used, and the sample is exposed to UV for up to 50s at a power of approx. 3mW/cm². At this stage, the photocurrent of the photodiode is measured, when the laser diode is operated in order to define a reference prior to the waveguide fabrication. Subsequently, the positions of the laser and the photodiodes are registered, the waveguide bundle configuration is defined, and the surface along the waveguide path is mapped by monitoring the intensity of the back-reflected light of a He-Ne laser with a photo diode in a confocal setup. Input and output of the butt joint waveguide bundle is referenced to a point at the laser- and the photodiode top edge, respectively. Taking into account the surface profile along the waveguide path and the coordinates of the start and end point of the waveguide bundle, the three axes stages move the sample such that the laser focus is scanned across the optical ORMOCER® layer in order to form a direct optical interconnect between the electro-optical components (Fig. 5). The feed rate of the axes is set to 20mm/min. Thus, the writing of the waveguides takes approx. 7 to 40 minutes, depending on the waveguide bundle configuration and the length of the bundle, respectively. After laser writing, the photocurrent is measured again and compared to the value before the inscription of the waveguides. Finally, the sample is thermally treated for 3 hours at 150°C to stabilize the complete system. At this state, the sample is ready for further processing such as lamination for terminating the PWB process (Fig. 6). A multilayer board with an embedded optical core layer is the final product.

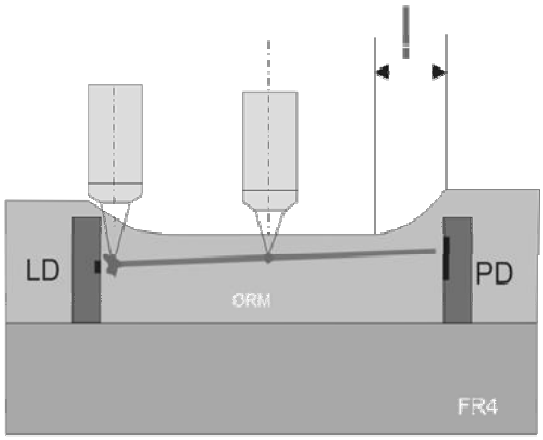

Fig. 5: Fabrication principle of directly written embedded waveguides. The exclamation point denotes the critical interface area between waveguide and diode chips, which is important for the coupling efficiency. At this location, the ORMOCER® film has to be planar and totally cover the diode chips. If there is a meniscus present in this region, the waveguide writing has to be compensated for a working butt joint between waveguide and diode chips.

3.4. Characterization of fabricated optical interconnects

The successful fabrication of a waveguide connection between laser- and photodiode was determined by the comparison of the light induced current of the photodiode before and after the waveguide writing. The ratio between the photocurrents with and without waveguide is in the range between 40 and 500. This yields a total optical loss of the system (including coupling losses at both waveguide caps and propagation loss) in the range 11-20dB, for a length of the waveguides of approx. 12 cm. The total damping of the waveguide is estimated to be approx. 7.8 dB. From earlier cut back measurements, it is found that the average loss of the ORMOCER® waveguides is approx. 0.64 dB/cm. This value is higher than the pure material loss, and is related to waveguide imperfections such as wall roughness or optical layer imperfections along the path of the waveguide. Nevertheless, such a system is capable of transmitting data at a transfer rate of >1Gbit/s with a bit error rate of 10^{-9}. Even higher data transfer rates of > 2Gbit/s using this approach are described elsewhere [13].

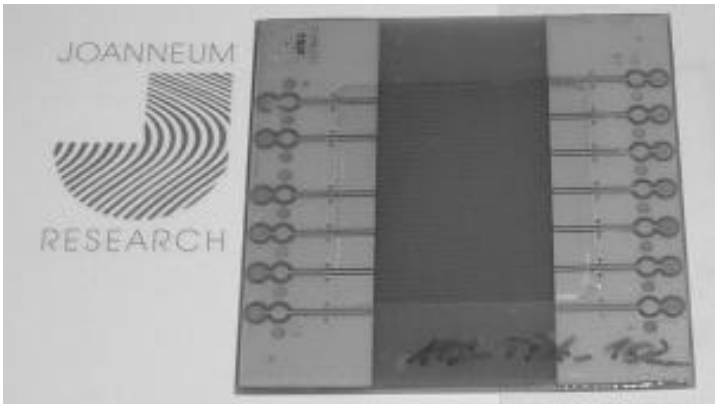

Fig. 6: 5x5 cm² PWB with attached frame, electro-optical components, and ORMOCER® film after the fabrication of the waveguides. At this stage, the PWB is ready for lamination, where the optical layer becomes a core layer of a multilayer board.

The above considerations are supplemented by cut-back characterization of the embedded waveguides. For this purpose, the sample is cut and grinded to different lengths. Light is coupled into the waveguide and at the output of the waveguide, the transmitted light is monitored by a CCD, and its intensity is determined (Fig. 7).

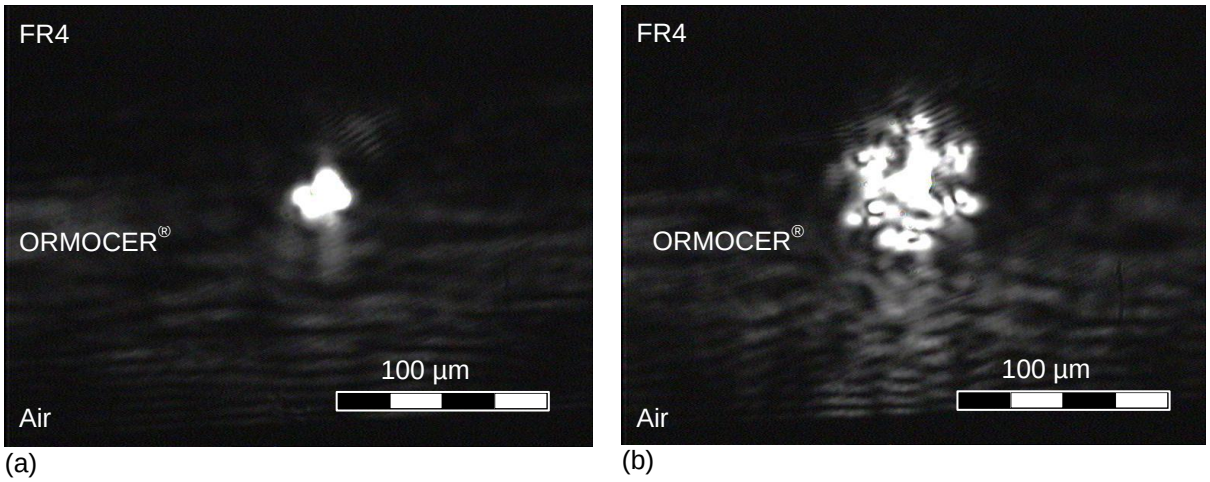

Fig. 7: (a) Transmitted intensity of a single line waveguide, and (b) transmitted intensity of a waveguide bundle with 1 center line and 6 satellite lines.

Three samples were investigated after different process steps. The transmission of the waveguides is measured at 10, 20, 25, and 30 mm. The optical loss of the single waveguide is approx. 0.43 dB/cm, and the loss of the bundle is approx. 0.65 dB/cm (Fig. 8, not thermally treated). Heating of the samples leads to an increased optical loss of the embedded waveguides. For thermally treated samples (150°C and 200°C for 3 hrs) the optical loss is estimated as <1.3 dB/cm.

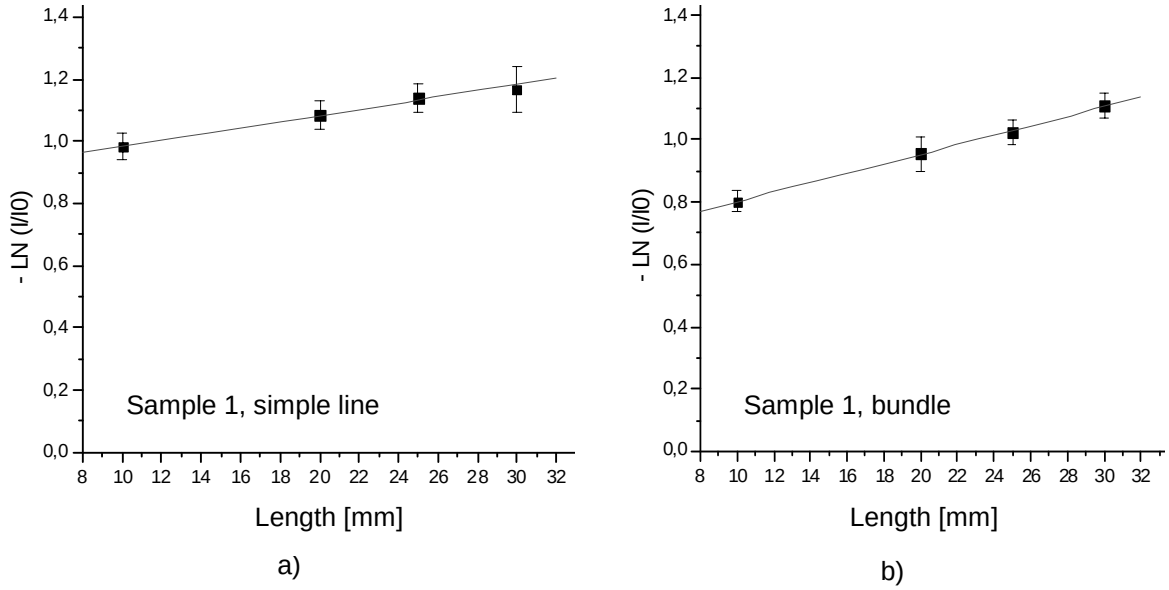

Fig. 8: (a) Cut-back measurement on a single line waveguide; the sample was characterized at various lengths and the optical loss of the waveguide was estimated to be (0.43 ± 0.09) dB/cm. (b) Cut-back measurement on a waveguide bundle; the sample was characterized at various lengths, and the optical loss of the waveguide bundle was estimated to be (0.65 ± 0.09) dB/cm.

3. SUMMARY

The two-photon 3D lithography with its inherent 3D capabilities, combined with a suitable inorganic-organic material, was successfully adapted and applied to the integration of an optical interconnect system into a printed circuit board. Several important requirements had to be faced from the material's and the technology's point of view. The ORMOCER® material had to be capable of forming both, the waveguide core and the waveguide cladding without the need for a two-material core-cladding system for embedded waveguides. In addition, the two photon-based laser writing method has the power that can create 3D structures within a material without the need of a layer-by-layer build up of a structure. The enormous flexibility of this lithographic method allows an implementation of machine vision capabilities including sample registration and surface mapping that are prerequisites to make the waveguide alignment and coupling a part of the waveguide fabrication process. Consequently, the entire board fabrication process is easier, and an industrial fabrication process of a leading edge multilayer PWB with an embedded optical layer becomes realistic. Hence, this method is considered very promising as a part of a large-scale fabrication process of PWBs, which pushes the versatility of such optically enhanced boards forward, and satisfies the increasing demand of faster intra-board communication. Joanneum Research in cooperation with AT&S are about to implement the described method into large scale industrial board fabrication processes.

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