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Editors

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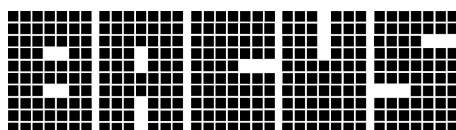

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Introduction

This proceedings volume contains accepted papers from the SPIE conference on Photomask Technology. The conference was arranged through the Bay Area Chrome Users Society (BACUS) and held as part of the 28th International Symposium on Photomask Technology 7–10 October 2008 in Monterey, California, USA.

The papers cover the most up-to-date research on emerging and ongoing issues facing the photomask industry in advanced lithography and their manufacturing solutions. With the deep sub-wavelength era upon us, the industry's progress will depend on the successful integration associated with optimization of design, mask making, and wafer fabrication. With respect to mask manufacturing infrastructure, topics are on advanced component processes, materials and patterning technologies for 32nm node and beyond. In addition to them, special components for optical extension technologies, DFM (Design For Manufacturing) technologies being coupled with EDA (Electronic Design Automation) are also captured. More advanced technologies for realizing emerging technologies such as EUVL (Extreme Ultraviolet Lithography) and nanoimprint lithography are also covered. Lastly business aspects that examine cost friendly and manufacturable solutions for our industry are reviewed as well.

This year's symposium continued the fine tradition of having wide international representation with a number of papers specifically as following;

- Mask Infrastructure
    - Mask Materials for Optical Extensions
    - Advanced Mask Processing and Materials
    - Patterning Technologies and Tools
    - Metrology
    - Defect Inspection
    - Defect Repair
    - Advanced Cleaning
    - Haze Contamination Control
- Mask Integrations
    - DPL (Double Patterning Lithography) Implementation
    - DFM
    - Simulation and Modeling
    - RET (Resolution Enhancement Technology) and OPC (Optical Proximity Effect Correction)/ORC (Optical Rule Check)
    - Wafer Plane Inspection
- Emerging Mask Technology
    - EUV Mask Processing and Substrates
    - EUV Mask Process Correction

    - EUV Mask Inspection
    - EUV Mask Repair
    - Masks for Nano Imprint
- Mask Business
    - Industry Assessment
    - Cost and Performance
    - Data Process Management

This year's Special Session was on the topic "Mask Infrastructure Challenges at 32 nm and Beyond," where industry experts from around the world spanning DFM, mask making (captive and merchant), equipments, wafer manufacturing, technology consultant, and national research institute met to explore the current most up-to-dated status and critical issues for the future. The summary of this session is provided by Griff Resor this year.

I thank all of the authors, particularly the keynote speaker Dr. Aart de Geus, Chairman and CEO of Synopsys, Inc. who gave us a talk with deep insight on this industry and prospect for the future which was so much instructive and stimulating. I also thank all the members of program committee for their dedication and hard work to help maintain the high quality of this conference with chairing respective technical sessions. Among this, I am especially grateful to my cochair Larry S. Zurbrick, Agilent Technologies, Inc. for all his help in making this year's symposium a great success. Of course, the sponsors who allow us to continue to attract talented speakers deserve recognition for without them, we would not be able to exist as a conference. Finally, I extend my sincere appreciation to the SPIE staff for their extensive efforts and their superb organizational skills that helped make this year's SPIE Photomask Technology conference a success, including a special thank you to SPIE for assembling and publishing this proceedings volume.

I hope you find the material comprehensive and valuable to your technical field, whatever that may be. BACUS is a professional society. If you are interested in what we are about, please visit the technical group on the SPIE website at www.SPIE.org/BACUSHome and join us as we continue to influence photomask technology development through our respected career applications.

Hiroichi Kawahira

Friday Special Session Schedule

Mask Infrastructure Challenges at 32nm and Beyond *

Chairs: **Larry S. Zurbrick,** Agilent Technologies, Inc. (United States); **Douglas J. Resnick,** Molecular Imprints, Inc. (United States); **Benjamin G. Eynon, Jr.,** Molecular Imprints, Inc. (United States); **M. Warren Montgomery**, CNSE/SEMATECH (United States)

Opening Remarks and Introduction
Larry S. Zurbrick, Agilent Technologies, Inc. (United States)

Mask Technology Perspectives

Software: Double Patterning and EUV Shadowing
Luigi Capodieci, Advanced Micro Devices, Inc. (United States)

E-beam PG: Resist, CD, CDU, IP, LWR
Shusuke Yoshitake, NuFlare Technology (Japan)

Pattern Transfer: CD bias, CDU, EPD
Thomas B. Faure, IBM Corp. (United States)

Inspection: E-beam versus Optical
Franklin D. Kalk, Toppan Photomasks, Inc. (United States)

Repair: Subtractive and Additive
Ted Liang, Intel Corp. (United States)

Metrology: CD, IP
Richard M. Silver, National Institute of Standards and Technology (United States)

Clean: Haze Issues etc.
Brian J. Grenon, Grenon Consulting, Inc. (United States)

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Optical Extensions: Double Patterning
Paul W. Ackmann, Advanced Micro Devices, Inc. (United States)

EUV: Blank, Defectivity, PT
Henry Yun, SEMATECH (United States)

Imprint: Write, PT, Inspection, Repair
Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

Open Discussion

* For materials relating to this session point your web browser to: www.SPIE.org/PM08
* For information about the BACUS technical group go to: www.SPIE.org/BACUSHome

Summary of the Friday Special Session

To 32nm and beyond: SPIE panel debates assortment of challenges *

What challenges must maskmakers overcome to reach the 32nm node, and what challenges lie beyond? The BACUS Program Committee assembled a panel of 10 experts to answer these questions. This glance at our future brought many people to this year's SPIE Photomask Technology Conference (Oct 6-10, Monterey, CA).

Luigi Capodiece of AMD launched the discussion with a lively review of EDA challenges. At the 32nm node, critical levels will be done with double or triple patterning. Manual methods are needed to decide which patterns go on each mask level. The design software then adds reticle enhancement (RET) detail based on tool and process models. The RET detail, sub-resolution assist features (SRAF) for example, can interact between mask levels. So careful simulation of this interaction is needed to avoid printing unwanted detail. More work by EDA suppliers is needed to make this work automatically; automatic routing is the most urgently needed capability.

Susuki Yoshitake of NuFlare described the company's work to develop adequate e-beam tools for mask writing. NuFlare clearly is supporting a large R&D effort; its most recent model EB 6000+ now meets 45nm node requirements, the model EB 7000 will be out next year (CY2009) for writing 32nm-node masks, and a model EB 8000 is planned for CY2011 for writing 22nm-node masks. As the data file size increases and the number of individual shaped spots increases; NuFlare expects to keep write time under 24 hours/mask. There are problems, though -- the company has been able to reduce the beam blur to less than 10nm, but current chemically amplified resist (CAR) then adds about 28nm of "process blur." So, an improved CAR with less diffusion blur and less line-edge roughness (LER) is needed.

The problem of mask etching -- transferring the e-beam resist pattern into the chrome mask -- was highlighted by Tom Faure of IBM. Each new node requires thinner resist, and the resist etch selectivity versus chrome is not good. Tom said the industry will need a new e-beam resist that can survive the chrome etch process -- some thought it might be more productive to work on the absorber material, to abandon chrome and move to dense MoSi or TaN. Etch loading and etch uniformity problems are also significant challenges. If these errors are stable in the etch tools, they can be offset in the design.

Inspection, repair and verification steps drive mask costs more than e-beam write time as the industry moves to higher resolution nodes, and Franklin Kalk from Toppan expects this trend to continue, though he finds inspection tools and repair tools are just keeping up with the challenge. The recent addition of good wafer plane inspection tools such as the Zeiss and Applied Materials AIM tools and new wafer plane simulation software from KLA-Tencor do sort out which defects will print, and can verify that repairs have been made correctly, but he is concerned that the very small market for these tools limits their availability. This is particularly true for EUV mask inspection and verification tools, though he said he was not yet ready to discuss this.

EUV mask inspection: Not if, but when?

Picking up the conversation on EUV masks, Ted Liang of Intel said that the Intel mask shop had all the tools that it needed to make working EUV masks except one -- Intel, and this industry, needs an EUV AIM tool. What's needed is a tool to help determine which defects really print -- but there is no supplier on the horizon. It is possible that the defect goal for EUV masks is tighter than it needs to be. Intel is also looking at ways to work around EUV mask defects; if mask blank defects can be mapped prior to e-beam exposure, it may be possible to shift or alter the pattern so that small defects will not print. An at-wavelength (13.5nm) AIM tool is needed to verify EUV masks are defect free before sending them to a production line. Liang reminded the audience that Intel is in 45nm volume production now and will be moving to the 32nm node next year, and the chipmaker wants EUV masks in CY2011 to be ready for production at the 16nm node in CY2013.

Henry Yun of SEMATECH predicted that EUV masks will be over 40% of advanced mask work in 2013 or 2014. He expects production using EUV masks will begin in earnest at the 22nm node. Progress on EUV sources and tools looks good (beta units should be in IC maker pilot lines in CY2009). EUV resist has made impressive progress this year, now that alpha tools and the LBNL Synchrotron are available to run tests. Mask defects are the most serious challenge, and Henry described SEMATECH's work in this area. Pits in mask blanks cannot be repaired, so work continues on blank polishing methods. Also, particle inspection tools continue to be improved; LBNL is building an actinic particle scanning capability, which will not be a production tool, but will enable correlation of optical and actinic detection methods. Another iteration of improvements is being made to the multi-layer coating tools. The level of mask defects can be reduced as quickly as the detection technology is improved. In addition, some work-around ideas are now being considered. Henry would like to see mask blanks come with alignment marks so that defect location can be known and the mask pattern moved and adjusted to compensate for defects. He closed by reiterating the need for an actinic AIM tool for EUV mask verification -- the availability of which, he lamented, is limited by commercial issues, not technology ones.

Haze, 3D, DP, EUV, NIL

Brian Grenon of Grenon Consulting described mask lifetime problems, with a map showing how haze formation on masks used in 193nm exposure tools is a global problem. As maskmakers have improved their cleaning process, it has become clear the problem is also a mask storage and lithography tool (fab environment) problem. And as maskmakers use more new materials such as MoSi, the chemical composition of haze changes to include these new materials, so the haze issue persists -- in fact, particles on masks now account for only about 33% of mask "defects," Grenon reported. He pointed out that as the industry moves to EUV the issue of thin organic films will be an even greater problem -- at 13.5nm any organic film will cause problems. Thus, mask "maintenance" costs will increase, he predicted, and the industry needs to consider this in their cost models as they look at the relative cost of different lithography choices.

Rick Silver of NIST reviewed CD and image placement metrology challenges, pointing out that the 3D shape of resist images is needed today, and 2D knowledge is insufficient. He believes optical scatterometry will be extendable through the 22nm node for CD measurement. His team continues to improve e-beam modeling of SEM behavior, and is adding surface charging effects to improve these tools (AFM continues to be their reference tool).

Paul Ackmann of AMD noted scanner makers are going to reach their overlay goals for double patterning, and are now putting the focus on masks which will be key to DP. He made a case for including more image placement measurement points within each die, which will enable higher order correction for overlay errors. He also shared some cost analysis presented earlier at the conference, showing that EUV will be more cost-effective than double patterning at the 16nm node.

Naoya Hayashi of DNP discussed making templates for nano-imprint lithography (NIL). Currently a 100 Kev single spot e-beam tool is used to write NIL template patterns -- which are about 50× too slow for volume production. With the single spot e-beam tool, DNP can make 15nm linespace patterns. With a 50Kev variable shaped beam (VSB) system, DNP has made very nice looking 24nm linespace patterns and 28nm dense contact and pillar patterns. Image placement errors are approximately 6nm 3σ over a mask area, and less over the 28mm × 24mm area needed for a 1X template. Incremental improvements in the e-beam writer, inspection, and repair tools are needed to meet tolerances for the 32nm node. Defects are an issue for 1X NIL templates.

Q&A: Cost concerns, EDA needs, NIL hurdles

Questions during the audience participation time reflected a keen interest in challenges of making EUV masks. None of the panel members had discussed

ways to manage EUV mask blank flatness and bending. Henry Yun noted that (a) the chuck will be made very flat so masks can be moved from tool to tool, and (b) electrostatic chucking will pull each mask flat. The residual unflatness and image placement errors due to mask bending will be modeled and corrected in the pattern data prior to pattern writing. (These issues had been covered in detail during on Thursday.)

Doug Resnick observed that defect data on EUV masks differed between the SEMATECH presentation and Intel presentation. Henry said his numbers reflect champion results and a scaling formula that SEMATECH uses to extrapolate EUV defects from measured optical detection tools. Ted Liang said he used average data for optically detected defects.

Is line-edge roughness (LER) an issue for masks? Ted Liang answered: Not really; the LER is not transmitted through scanner lenses. This is really a wafer level issue.

Greg Hughes asked if the IMS ion mask exposure Tool (iMET) could be used as a mask writer, and that is the plan; IMS presented their results on Tuesday. (By using multiple beams of hydrogen ions, not electrons, IMS can expose non-CAR resists at a sufficient rate; they showed excellent results at 16nm.) The IMS presentation included an announcement that IMS and NuFlare will establish a joint development project to build an ion multi-beam mask exposure tool.

There was an audience challenge regarding EUV mask cost expectations. Brian Grenon anticipates hydrocarbon contamination between multi-level coating layers may cause EUV mask yield and lifetime problems. Franklin Kalk expects EUV blank cost to go up, and EUV mask yield will drop. Franklin added that as the industry adopts double patterning added benefits will be discovered, making it more cost-effective for a longer time (which has been the history of similar advances). Kalk observed that each year the EUV crossover point moves out; SEMATECH's Yun agreed with the schedule slip, but added that he expected EUV blank cost to come down and yields to improve as volume increases (typical for a learning curve). Clearly this issue will be a hot topic at future BACUS meetings.

Warren Montgomery of SEMATECH observed that it was time for maskmakers to "share the pain" by adopting better resists. Brian Grenon added, "And new absorber materials" to improve the etch process and mask lifetime.

More back-and-forth from the audience participation segment of the program:

- AMD's Ackmann reminded everyone that equipment costs drive mask costs. Tools for writing, inspecting, repairing, and verifying are expensive and have a low throughput.

- Was there a chance that the EDA task would get simpler with EUV? "No," replied Luigi Capotieci of AMD; EUV masks will need OPC and verification, which translates into lots of computing time. Liang of Intel observed that once maskmakers find a good trick (e.g., RET) they don't abandon it. Ideas presented earlier about defect mitigation (moving and altering patterns to cover up defects) would increase computing needs.

- Since a defect free mask seems impossible, how many defects might be tolerated? 100 defects may be OK, if they are small, Ted Liang answered.

- Why isn't NIL in production (for ICs)? Throughput is only at 4wph; overlay is at 15nm. Inspection and repair infrastructure is not ready. The risk of repeating defects on the production line also needs to be addressed. How can people monitor for such problems and remove a template for cleaning when a printing defect is observed?

From this panel discussion it seems maskmaking infrastructure for the 32nm node is nearly ready for production, since there were few questions regarding this. The audience was much more interested in their next challenge, EUV masks. This is progress -- clearly this audience has accepted that EUV source and resist technologies are moving at the right pace toward production. As this group turns its attention to EUV maskmaking, it appears the IC industry will finally adopt EUV for some layers at the 22nm node and for many more layers at the 16nm node. This is Henry Yun's expectation. He may be right this time.

Griff Resor

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