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CMOS SENSORS FOR ATMOSPHERIC IMAGING

Jérôme Pratlong[1], David Burt1, Paul Jerram[1], Frédéric Mayer[2], Andrew Walker[1], Robert Simpson[1], Steven Johnson1, Wendy Hubbard[1]
[1]e2v technologies, Waterhouse Lane, Chelmsford, Essex, CM1 2QU, UK ; [2]e2v semiconductors, avenue de Rochepleine, BP123, 38521 Saint Egrève, France

I. INTRODUCTION

Recent European atmospheric imaging missions have seen a move towards the use of CMOS sensors for the visible and NIR parts of the spectrum. These applications have particular challenges that are completely different to those that have driven the development of commercial sensors for applications such as cell-phone or SLR cameras. This paper will cover the design and performance of general-purpose image sensors that are to be used in the MTG (Meteosat Third Generation) and MetImage satellites and the technology challenges that they have presented.

We will discuss how CMOS imagers have been designed with 4T pixel sizes of up to 250 µm square achieving good charge transfer efficiency, or low lag, with signal levels up to 2M electrons and with high line rates. In both devices a low noise analogue read-out chain is used with correlated double sampling to suppress the read-out noise and give a maximum dynamic range that is significantly larger than in standard commercial devices.

Radiation hardness is a particular challenge for CMOS detectors and both of these sensors have been designed to be fully radiation hard with high latch-up and single-event-upset tolerances, which is now silicon proven on MTG. We will also cover the impact of ionising radiation on these devices.

Because with such large pixels the photodiodes have a large open area, front illumination technology is sufficient to meet the detection efficiency requirements but with thicker than standard epitaxial silicon to give improved IR response (note that this makes latch up protection even more important). However with narrow band illumination reflections from the front and back of the dielectric stack on the top of the sensor produce Fabry-Perot étalon effects, which have been minimised with process modifications. We will also cover the addition of precision narrow band filters inside the MTG package to provide a complete imaging subsystem. Control of reflected light is also critical in obtaining the required optical performance and this has driven the development of a black coating layer that can be applied between the active silicon regions.

II. LARGE PIXELS

The METimage project has the objective of providing space-based meteorological predictions. The sensor is to be front-illuminated, with the option of back-illumination at a later date. The pixel pitch is very large at 250 µm × 250 µm The basic four-transistor (4T) architecture with a pinned photo-diode, transfer gate, detection node C_N and source-follower buffer amplifier has been chosen to meet the low noise requirement as this arrangement enables kTC noise cancelling by means of correlated double sampling. A test chip has been produced to validate the pixel design and the read-out circuitry; this is designated type CIS116. The reported results are from this device.

Such a large pixel is a challenge in terms of design issues with minimal polysilicon, active and metal densities, and the physics of transferring carriers over large distances without significant transit-time lag. Due to the foundry's density rules and charge transfer issues, using just one photodiode per pixel is not an option. Instead the main diode has been split into 8 sub-photodiodes each 115.9µm x 52.5µm and each with a separate transfer gate. All 8 sub-photodiodes outputs are then binned together at a common sense node, as shown in Fig. 1.

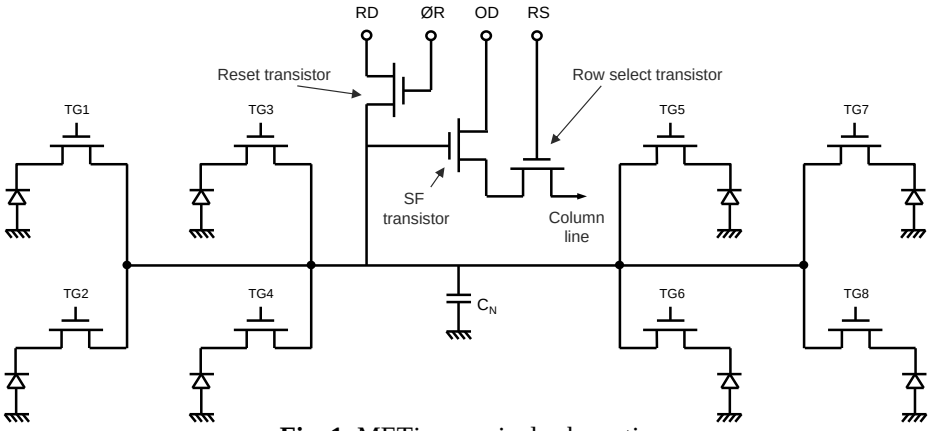

Fig. 1. METimage pixel schematic

Eight different versions of this pixel were designed as follows. Either one or two transfer gates located on the horizontal (H) or vertical (V) sides of the photodiode, and with two variants having extra capacitance added to the sense node to reduce the charge-to-voltage conversion factor (CVF) and thereby increase the charge handling capacity. In all cases extra transfer channels are diffused into the photodiode structure. These have a gradually increasing channel width which causes a voltage gradient along the length of the channel to drift the electrons towards the output, which is much faster than the normal diffusion through a uniform diode. Finally, two other variants have a two level implant scheme for the channels allowing a supplementary boost in transfer time.

Tab. 1 gives the design details of the pixel variants and the measured performance parameters.

	TG	Extras	CVF ($\mu V/e^-$)	N_O(max) (ke^-)	QE (650nm)	V_{SO}(max) (V)
Variant 1	1V		3.11	604	53.6%	1.88
Variant 2	2V		1.97	970	52.7%	1.92
Variant 3	1H		0.72	2505	47.8%	1.81
Variant 4	2H		0.95	1987	47.7%	1.90
Variant 5	1V	+ C_N	1.20	1495	54.1%	1.79
Variant 6	2V	+ C_N	0.76	2425	43.6%	1.84
Variant 7	1V	+ Imp	3.12	597	53.0%	1.86
Variant 8	1H	+ Imp	2.03	950	50.3%	1.93

Tab. 1. Pixel variants

V_{SO}(max) is the maximum output signal in volts. N_O(max) is the corresponding maximum signal in electrons given by V_{SO}(max)/CVF. QE is the maximum quantum efficiency at $\lambda \sim 650$ nm averaged over a 100 nm window. The CVF with the horizontal transfer gates is lower than that of the vertical transfer gates because the extra tracking adds more capacitance to C_N.

Fig. 2 shows that the lag performance is extremely good with all pixel variants.

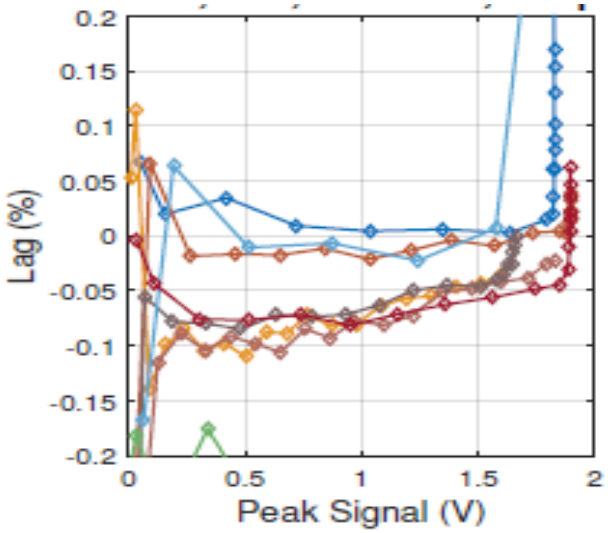

Fig. 2. METimage pixel lag (all variants)

The measured noise in the dark is found to be very similar in all variants, namely 120 µV rms from a low-noise video output or 300 µV rms using a circuit capable of driving a large external load, as expected in some applications. As the peak output voltages are also very similar, the dynamic range using the low-noise output is typically 84 dB and that using the large load drive circuitry is 76 dB.

III. RADIATION_HARD DESIGN

A. Overview

The MTG sensor (CIS111) [1] has 5 independently-operated channels of large rhombus shaped 4T pixels operating at different wavelengths between 414 nm and 924 nm, as shown schematically in Fig. 3. The inner block has about 50 µm square pixels arranged as 448 × 4 arrays. Each of the four outer blocks has about 100 µm square pixels arranged on a staggered format of 224 rows and 4 columns. The layout of the rhombus shapes gives an effective pixel pitch that is smaller than the photodiode pitch; this is important for maximizing spatial resolution (MTF). The output circuits have CVF values between 0.83 µV/electron and 7.53 µV/electron to suit the signal levels to be generated by the anticipated illumination levels. There is on-chip circuitry to select one of the four columns in each row on read-out at 4 MHz.

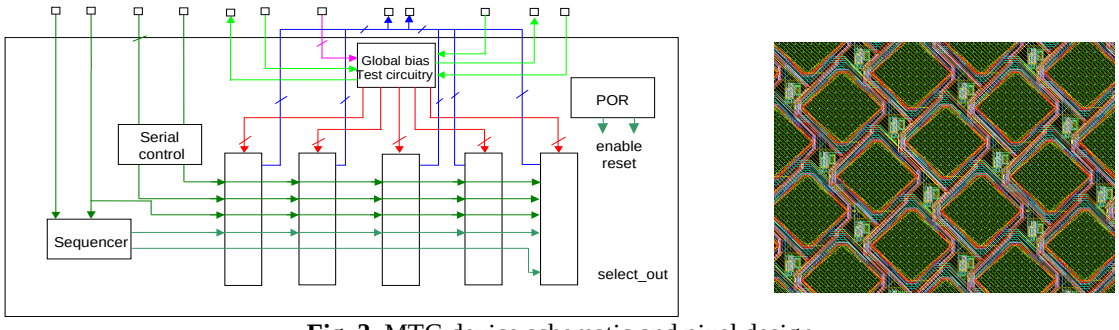

Fig. 3. MTG device schematic and pixel design

B. Ionizating effect

In the context of MTG program a shuttle was manufactured with 4T type large pixel variants to prove the concept. The variants included photodiodes with one or two transfer gates as well as sense node conversion capacitance of different nature (diffusion, MOS capacitance or MIM capacitance). Two photodiode sizes were developed a HR (High resolution) pixel of about 30µm x 50µm and a FD (Full Disk) of about 100µm x 100µm. The pixel schematic is shown Fig. 4 and the variants are reported Tab. 2.

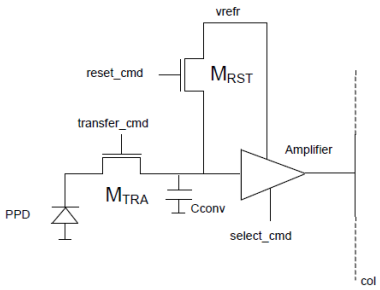

Fig. 4. MTG-FCI pixel schematic.

Variants	Number of transfer gate	Extra capacitance type
FD1	2	None
FD2	1	None
FD3	2	MIMCAP
FD4	2	MOSCAP
FD5	1	MOSCAP
HR	2	MOSCAP

Tab. 2. Pixel variants.

Several devices have been irradiated with Co60 source in CEA Saclay. The radiation conditions are given in Tab. 3 below:

Device	Radiation rate	Duration	Total dose	Polarisation/Electrical bias
C3W5	10.11 krad/hour	4h57	50krad	ON
C5W5	4.2 krad/hour	4h46	20krad	ON
C6W5	10.11 krad/hour	4h57	50krad	OFF
C4W5	N/A	N/A	N/A	Reference

Tab. 3. Radiation conditions.

The behavior of performance up to 50krad range shows that:

- Radiation impact on CVF is negligible.
- Mean dark current increases with gamma radiation (~ ×18 after 50krad(Si)) but remains at a low level (~50pA/cm^2) much lower than the specification.
- The dark current behaviour with temperature (doubling factor) is not affected by radiation.
- As is often the case, the dark signal non-uniformity also increases but within a smaller proportion than Dark Current (~ ×6 after 50krad(Si)).
- Total read-out noise also increases but within a moderate proportion (~+15%).
- On the large FD type pixels, lag worsens after radiations but still remains lower than the design specification except for FD2 variant (one transfer gate) for which the lag remains below the design goal but slightly exceed the specification. The lag remains almost immeasurable for the smaller HR type pixel.

- Linearity at high levels is a slightly affected after radiation especially for the pixel variant with only one transfer gate (FD2).

Single Event Effect (SEE)

Another concern for CMOS radiation tolerance is the immunity to SEE including Single Event Latch-up (SEL), Single Event Transient (SET) and Single Event Upset (SEU). As part of the MTG validation program [2], Heavy Ion tests have been performed on a flight model configuration to evaluate its SEE immunity.
Usually, the SEE is categorized in:

- Non-destructive
  - Single event upset (SEU) – change of logic state in memory element.
  - Single event transient (SET) – transients in circuit that lead to erroneous data being captured.
  - Single event functional interrupt (SEFI) – temporary loss of device functionality (for an imager of this simplicity, this is caused by bus contention).
- Potentially Destructive
  - Single event latch-up (SEL) – a parasitic thyristor causes circuit lockup or catastrophic failure.

The MTG device is designed with features to mitigate against these SEE types:

- Triple mode redundancy (TMR), see Fig. 5 (to address SEU)
- Big transistors with large drive and capacitance (to address SET)
- Big global clock buffers with high output capacitance (to address SET)
- Layout considerations and guard rings around all wells (this is
- to address SEL)

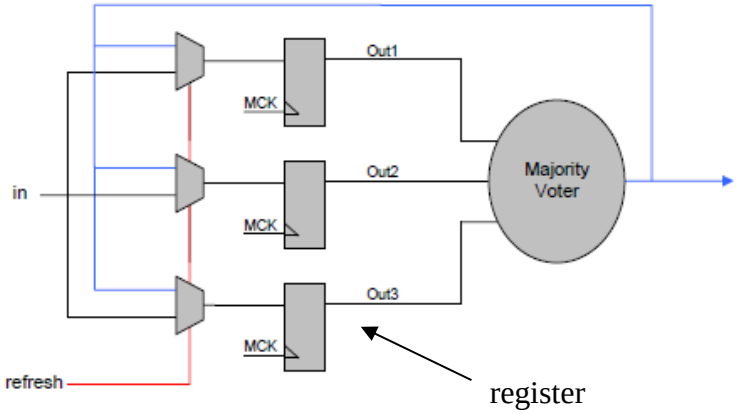

Fig. 5. TMR implementation example.

The TMR was implemented with two types of register depending on how critical SEU is for a given function:

- Rad-hard
  - Implemented for all digital control functions except for the SPI
  - TMR refreshed at 4 MHz rate
- Low power
  - Less radiation hard
  - Implemented for the SPI
  - TMR refreshed at 2.6 kHz rate

The low power register has half the consumption of the rad-hard version and needs half the silicon area. Note that the size of the rad-hard register is considerably bigger than the low power version.

The Heavy Ion tests [2] have been carried out at the facility of Universite Catholique Louvain (UCL), Belgium using the CYCLONE facility. This is a multi-particle variable energy cyclotron. Two cocktails of heavy ion species were available for SEE testing: a high energy cocktail for good range in silicon and a low energy cocktail which has a greater stopping power. Each cocktail consists of several ion species which have similar M/Q (mass/charge state) values.

No SEL was observed at the highest LET and at the maximum flux, so it was concluded that the SEL threshold was greater than 67.7 MeV cm^2 mg^{-1}. This was confirmed on two sensors over several test runs. This includes both non-destructive and potentially destructive SEL. It is also worth noting that no other high current state was observed due to SEFI at a LET of up to 67.7 MeV cm^2 mg^{-1}.

The SEU was also investigated on digital circuitry using: Rad-hard Shift Register – Used for Integral Sequencer and Timing and Readout Functions

Ion species	Tilt Angle [°]	Effective LET [MeV cm^2 mg^{-1}]	Effective Flux [$cm^{-2}s^{-1}$]	Effective fluence [cm^{-2}]	Number of Errors
$^{132}Xe^{26+}$	0	67.7	5e3	2.1e6	0
$^{84}Kr^{17+}$	0	40.4	5e3	2.1e6	0
$^{84}Kr^{26+}$	60	65.3	7e3	1.21e6	1

Tab. 4. conditions and results for the digital circuitry using TMR with rad-hard flip-flop

In conclusion, the threshold LET is about 65 MeV cm^2 mg^{-1} (although the exact position is not clear). But the saturation cross-section is not measurable due to high LETth. In order to accurately determine Cross-section vs. LET characteristic it would require ion species with LET > 67 MeV cm^2 mg^{-1}.

Low-Power Shift Register – Used for Serial Programmable Interface

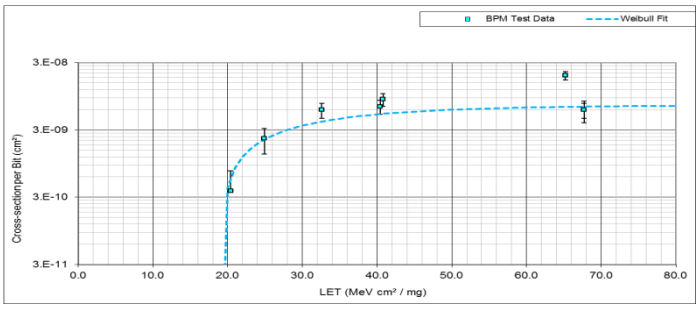

Fig. 6. Low power register SEU cross-section.

The low power shift register is less rad-hard than the other shift register type on this imager. The results confirm that using smaller transistor dimensions for lower power consumption lowers the LET threshold. A refresh rate for TMR of 2.6 kHz rather than 4 MHz also has an impact on the cross-section. In conclusion, the digital circuitry using a low power register has a LETth of 19 MeV cm^2 mg^{-1}.

It was possible from this radiation campaign to propose a worst case analysis to estimate the in-orbit SEE rates for latch-up and upsets. The good results does not give enough information for a full cross-section vs. LET curve, instead a step function is used with the step at LETth. The results are reported Tab. 5.

	LETth (MeV$cm^2$$mg^{-1}$)	Mission rate (day^{-1})	Reliability over 8.5 years (%)	Comments
SEL	> 67.7	< $2x10^{-6}$	99.2	This worst case as no latch-up was actually observed
SEU rad-hard register	65	< $4x10^{-12}$	99.9999	Sequencer, timing and readout control
SEU low power register	19	< $1x10^{-8}$	99.996	Serial programmable interface

Tab. 5. Predicted SEE rate

IV. SPECTRAL RESPONSE

A. Etalon effects

In front-illuminated CMOS sensors the photodiode is generally covered with a layer of dielectric material that provides passivation and protection. Since this material is also used for insulation between the various metal layers used for supplies, clocks and interconnections, the type of dielectric and the total thickness can vary depending on the process used by a foundry to fabricate devices. A consequence of using this structure is that the spectral response can show pronounced peaks and troughs at wavelengths where the incident light is either in-phase or out-of-phase with the light reflected back from the silicon surface. The modulation depth between the maxima and minima is dependent on the refractive indices of the dielectrics in the stack and the separation between the peaks reduces as the overall thickness increases. Furthermore, the modulation depth tends to be a minimum if the refractive indices gradually increase from air to silicon but a maximum if any layer has an index higher than the layer below it. This latter case was the situation with the process initially used by the foundry to fabricate our MTG devices. The dielectric stack was about 5 µm of silicon dioxide, index ~ 1.5, covered by a layer of silicon nitride, index ~ 2.0, for passivation purposes. At mid-range ($\lambda \sim 650$ nm) the peaks and troughs were in the region of 90% and 40%, as shown in Fig. 7, with a separation as expected for the total thickness. It may be noted that the drop-off in response at the shorter wavelengths is largely through losses associated with the surface p+ layer and that at the longer wavelengths is due to the finite active thickness of the silicon.

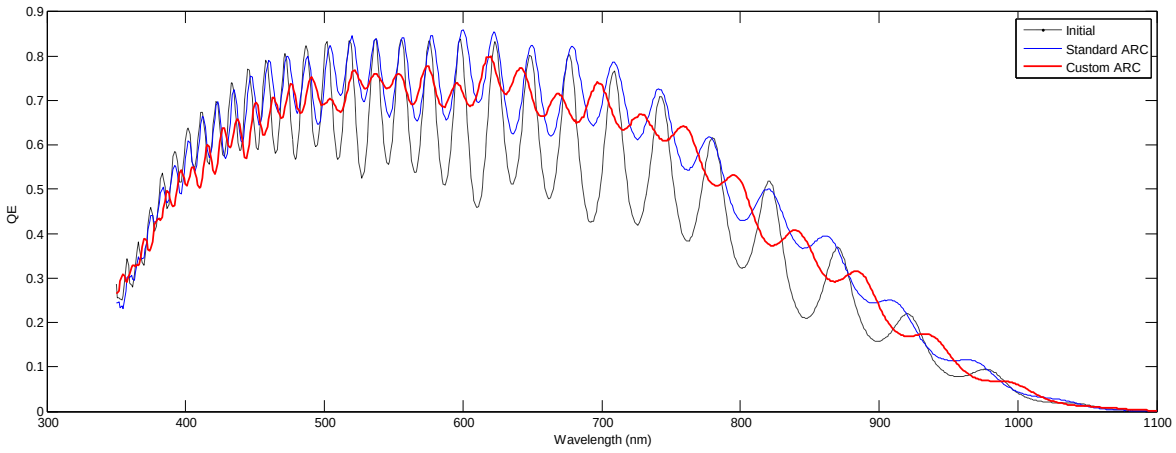

Fig. 7. Measured spectral response with and without antireflection coatings (100% fill-factor)

As a first attempt at improvement devices were fabricated without the nitride layer; this reduced the modulation depth but had the unfortunate result of an increase in the background dark current. Some form of passivation is therefore required, but with dielectrics having the required refractive indices. These layers are equivalent to those used in optical components to reduce reflection, i.e. anti-reflection coating or ARC, and are therefore described as such. Results using the foundry's standard ARC and then a custom optimized version are also shown in Fig. 7 for test devices having 100% fill-factor. The optimized version is clearly superior with the modulation depth no higher than about 10% and it is this version being used for current manufacture.

B. Filters

The MTG sensor (CIS111) is describe in section III. More detail has been reported[1]. e2v fully assembles the devices in a package that includes a ribbon flex connection, custom optical filters and a permanent window, as shown in Fig. 8.

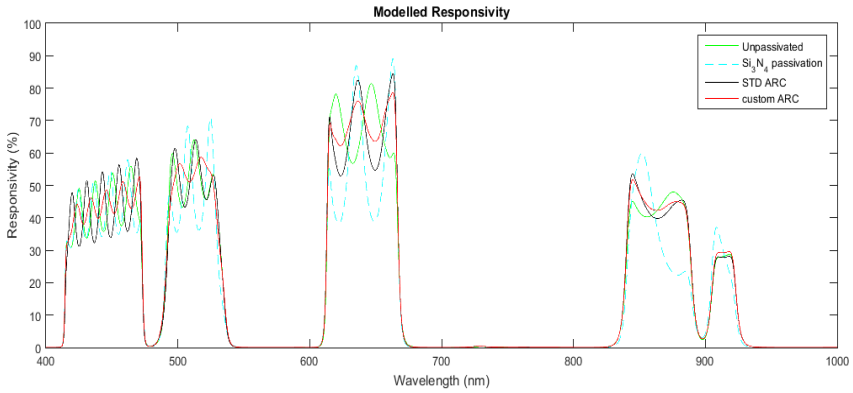

Fig. 8. Packaged MTG device

It was important to assess the optical performance including the filters to guarantee the overall performance. A total system QE including the filters is reported below.

V. BLACK COATING

There are quite a level of metallization between channels of MTG-FCI devices (see section 3.1) in order to route signals, readout path and supplies. This metallization will cause reflection which can cause, in a sensor chip imaging, artefacts and are best eliminated. Avoiding these reflections is however possible with a black coating having a low reflectivity over most of the visible band of wavelengths, as shown in Fig. 9.

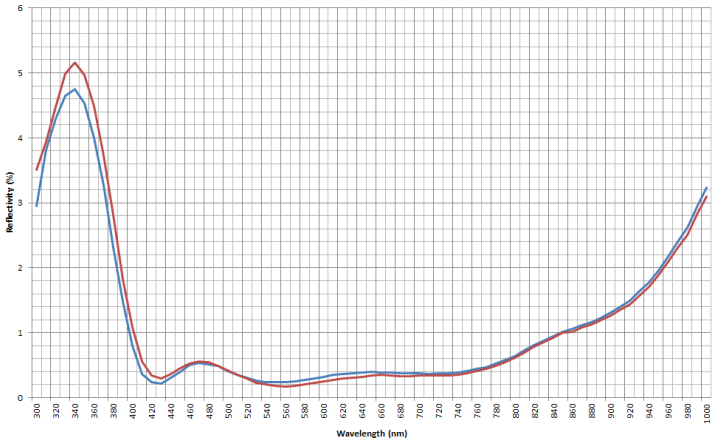

Fig. 9. Black coating reflectivity

VI. CONCLUSIONS

The behavior of two general sensors used for atmospheric imaging was presented. The results reported shown how challenges have been dealt with obtaining good performances such as extremely low lag (<0.2%) on a very large pixel of 250 µm × 250 µm, reducing etalon effect and reflectivity by developing ARC and black-coating processes and building designs immune to SEL and extremely robust to SEU.

VII. REFERENCES

[1] Pike, A TAS et al "Workshop CMOS Image Sensors for High Performance Applications - CNES - 26th & 27th November 2013," CNES workshop 2013.
[2] Simpson, R et al, "High SEE Tolerance in a Radiation Hardened CMOS Image Sensor Designed for the Meteosat Third Generation FCI-VisDA Instrument," CNES workshop 2015