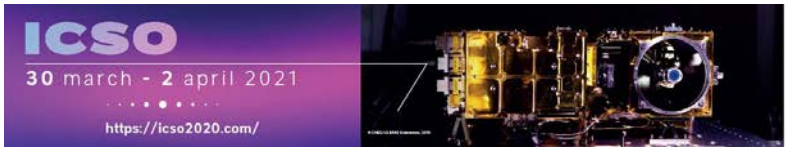
International Conference on Space Optics—ICSO 2020

Virtual Conference

30 March–2 April 2021

Edited by Bruno Cugny, Zoran Sodnik, and Nikos Karafolas



The H2020-SPACE-ORIONAS project: "Lasercom-on-chip" for high-speed satellite constellation interconnectivity

International Conference on Space Optics — ICSO 2020, edited by Bruno Cugny, Zoran Sodnik, Nikos Karafolas, Proc. of SPIE Vol. 11852, 118521L · © 2021 ESA and CNES
CCC code: 0277-786X/21/$21 · doi: 10.1117/12.2599248

The H2020-SPACE-ORIONAS Project "Lasercom-on-chip" for High-speed Satellite Constellation Interconnectivity

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ABSTRACT

H2020-SPACE-ORIONAS is a 3-year Research and Innovation Action program funded by the European Commission focusing on the development of compact optical transceiver and amplifier modules applicable to new generation optical inter-satellite links. ORIONAS explores photonic integrated circuits and small form factor fiber optics leveraging their success in datacenter interconnect and hi-rel aerospace applications to deliver miniaturized modules and devices that can shrink considerably the SWaP of lasercom terminals. This paper presents the most recent project achievements.

Keywords: optical inter-satellite links, satellite constellations, photonic integrated circuits, small form factor optics.

1. INTRODUCTION

Laser communications are gearing up for their entry into satellite constellations. The high volume of satellites required to provide a global coverage and at the same time the small physical size of each satellite impose stringent requirements on the cost, size, weight and power consumption (C-SWaP) of the on-board laser terminals. The current laser modem generation is built with discrete transceiver and amplifier components and as such systems are still bulky and complex. New generation laser modems are expected to merge fiber optic and electronic elements on nano-photonic circuits that can be fabricated within semiconductor foundries just as electronic circuits are fabricated today for any high-volume consumer-based application. ORIONAS is a H2020-SPACE research project that aims to provide a photonic technology platform that will disrupt both the shape of lasercom modems as well as the way they are built and tested making a drastic impact on the system C-SWaP. ORIONAS invests in monolithic integration within European BICMOS and InP foundries to leverage cost-effective access to high performance technologies and squeeze the key transceiver and amplifier elements that constitute the laser modems into integrated circuit areas of a few mm^2. Leveraging electronic-photonic integration and using hi-rel small form factor fiber (SFF) optics the project intends to demonstrate a cost-effective solution for photonic devices that will deliver 25 Gb/s data rates on a single channel. In this paper we report the system architecture and the project progress on the development of transceiver PICs and sub-assemblies.

2. SYSTEM ARCHITECTURE

2.1 Optical link specifications

The primary application target is OISLs within satellite constellations. In this scenario four laser terminals are deployed on-board the satellite to realize inter-plane and intra-plane links. Each of these terminals supports both transmit and receive channels. Separation between transmit and receive channels are preferably achieved through wavelength allocation in two separate sub-bands. As shown in the figure below, Blue and Red sub-bands are separated by a significant guard band. This approach calls for two versions of terminals, so-called Blue and Red terminals, i.e. terminals emitting respectively in Blue and Red sub-bands.

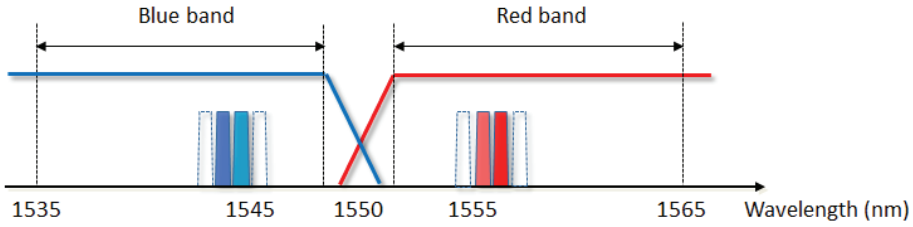

Figure 1: Typical OISL wavelength allocation for bi-directionality

The optical link configuration in terms of operating wavelength, data rate and distance is as follows:

- Operating wavelength (for communication) is 1.55 µm, C-band,
- Data-rate : 20 – 50 Gb/s range,
- Full-duplex/bidirectional capabilities are required with symmetric throughput,
- Data rate adaptability might be desired in some applications, but it is assumed that optical link devices will be designed for a certain fixed line rate,
- Target distance is spanning from 1000 to 6000 km depending on link type (intra- vs. inter-plane) and constellation geometry, as better shown in the figure below.

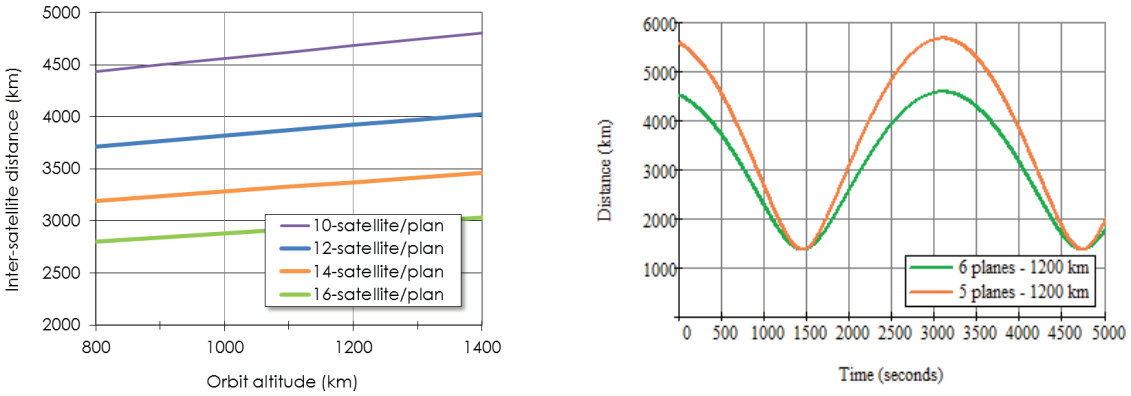

Figure 2: Intra-plane (left) and inter-plane (right) Optical Inter-satellite Links (OISL) distances in typical LEO satellite constellations

The Table below provides an exemplary link budget analysis for an inter-plane OISL of 6000 km maximum distance supporting 25 Gb/s and operating with DPSK modulation and optically pre-amplified direct detection. The optical launch power is estimated to be +32 dBm and the receiver sensitivity is -41 dBm for a BER of 10^{-4}.

Table 1 Preliminary link budget for inter-plane OISL with 25 Gb/s DPSK

Link parameter	Level	Unit	Note
Optical **launch** power	+32	dBm	
Power sharing	0	dB	1 channel
Tx telescope path losses	-4	dB	including obscuration
Radiated power/channel	+28	dBm	
Tx telescope gain	107.7	dB	12 cm aperture diameter
Tx depointing losses	-1.7	dB	@ +/ - 5 µradians
Free-space losses (dB)	-273.7	dB	@ 6000 km distance
Rx telescope gain	107.7	dB	12 cm aperture diameter
Received power/channel	-32	dBm	
Rx telescope path losses	-3	dB	including obscuration
Fiber coupling loss	-4	dB	single-mode fiber coupling
Fiber coupled power	-39	dBm	
Rx sensitivity (10^{-4} BER)	-41	dBm	optically-preamp. DPSK @25 Gb/s (10^{-3} BER)
Link margin	2	dB	

2.2 Physical layer architecture

The schematic below illustrates the physical layer architecture of the optical inter-satellite link (OISL). The system provisions one “main” channel to deliver 25 Gb/s data rate, whereas a second channel is used for redundancy or to double the aggregate data rate to 50 Gb/s if required. The system schematic shows both directions of the OISL, denoted as “downstream” (dashed line) and “upstream” (dotted line) directions. For illustration purposes the schematic depicts only the “downstream” optics in detail – the “upstream” optics will be an exact replica of the “downstream” optics. The schematic identifies the basic building blocks of the transmission link and the main device interfaces. Further detailed analysis of the interfaces per photonic module is provided in the sections below. The yellow boxes indicate the modules that will be assembled and integrated in ORIONAS. The blue lines indicate optical interconnections, whereas the black lines indicate electrical interconnections.

Optical
Electrical (RF or DC)

Tx_MD Transmitter module
Tx_RF RF ceramic - transmitter
Tx_EPIC Transmitter electronic-photonic circuit
LD Transmitter laser diode
HP_SOA High-power SOA
PBC Polarization Beam Combiner
TEL Telescope
LNOA Low noise pre-amplifier
Demux Wavelength demultiplexer

Rx_MD	Receiver module
Rx_EPIC	Receiver electronic-photonic circuit
Rx_RF	RF ceramic - receiver

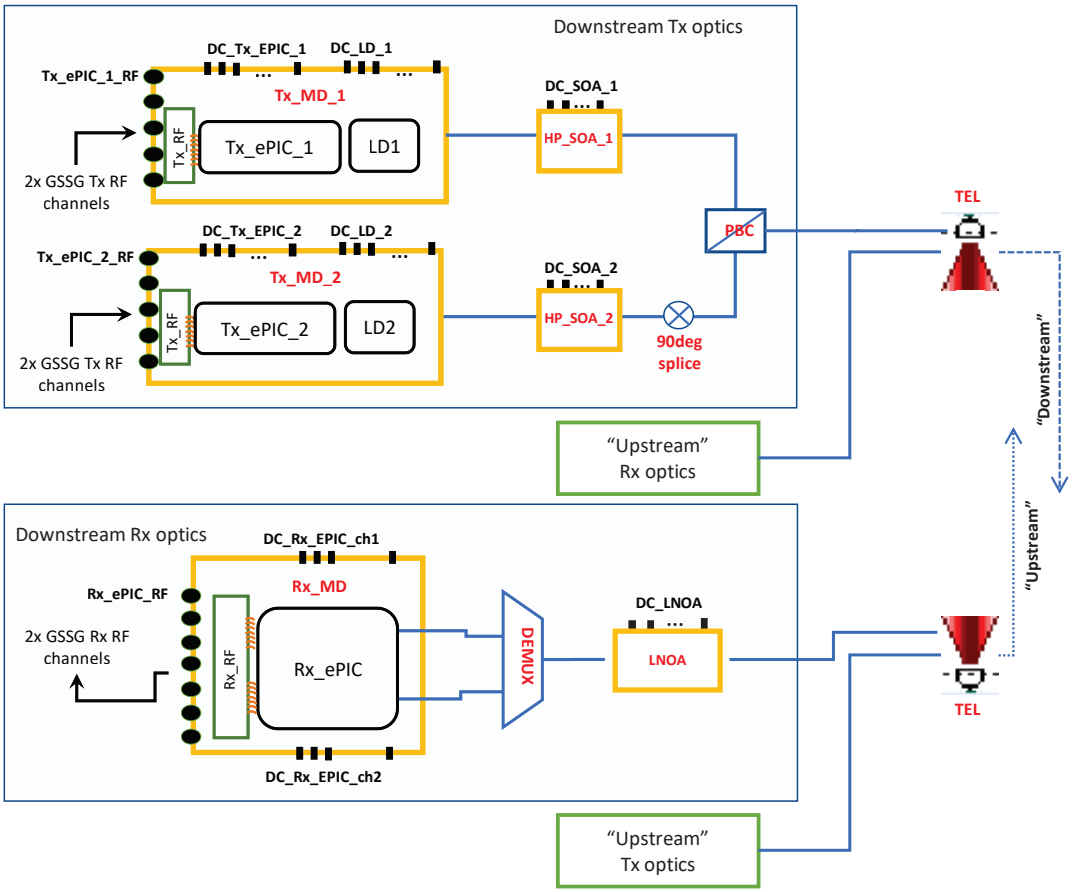

Figure 3: ORIONAS OISL architecture

The main elements of the laser modems depicted in the figure above are:

- Two single-channel transmitter modules (Tx_MD) each delivering 25 Gb/s data rate. Each Tx_MD contains the seed laser diode (LD) and the Mach-Zehnder modulator/driver electronic photonic integrated circuit (Tx-ePIC).
- Two discrete high-power semiconductor optical amplifier modules. Each HP-SOA delivers an optical output power in the range of +30 dBm. Each HP-SOA module contains the SOA CoC and the associated optical coupling and thermo-electric cooling elements.
- Polarization Beam Combiner. The PBC is used to multiplex the two data signals in the same fiber through polarization multiplexing. Alternatively a WDM multiplexer can be used.
- A twin-channel receiver module (Rx_MD) with each receiver being a polarization diversity receiver which demodulates and detects one randomly polarized 25 Gb/s DPSK modulated signal. The Rx_MD contains a monolithic twin array of receiver electronic photonic integrated circuits.

- One twin-channel low noise optical fiber amplifier. The LNOA amplifies the data signals and launches the amplified signal to the DEMUX.
- A twin-channel optical demultiplexer. The Demux is coupled to the Rx_MD for further optical detection. It is used to separate the two wavelength channels into different optical fibers.

The sections below focus on the development of the transceiver circuits and sub-assemblies.

3. INTEGRATED OPTICAL TRANSCEIVERS

3.1 Functional diagrams

The figures below illustrate the functional diagrams of the DPSK transmitter and receiver modules.

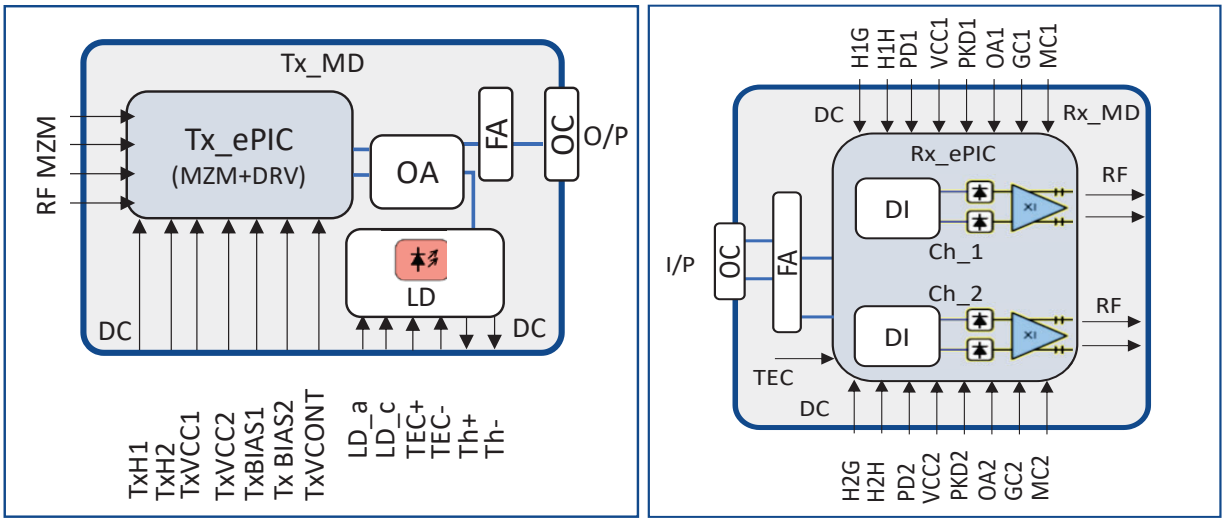

Figure 4: Functional diagram of the (left) integrated DPSK transmitter module and (right) integrated DPSK receiver module. (black arrows: electrical, blue lines: optical). The modulator and receiver EPIC circuit are outlined within the grey areas.

With reference to the functional block diagram shown above, the DPSK Tx module (Tx_MD) includes the following basic functional components:

- One Mach-Zehnder modulator (MZM) integrated with its driver (Tx_ePIC)
- One laser diode (LD)
- One optical adapter (OA)
- One fiber assembly (FA)
- One optical output connector (OC)

The module interfaces are:

MZM RF interfaces:

a) The MZM is driven by the RF differential data signal (GSSG configuration).

MZM DC interfaces:

a) DC supply voltage to modulator driver (TxVCC1 and TxVCC2)

b) DC bias voltage to modulator driver (TxBIAS1, TxBIAS2)

c) Control voltage for gain control (TxVCONT)

d) Thermal tuning for operational point adjustment (TxH1, TxH2)

LD DC interfaces:

a) LD driving current through the anode and cathode (LD_a, LD_c)

b) LD temperature control through the thermo-electric cooler (TEC+/-)

c) Temperature reading through the thermistor (Th+/-)

The DPSK Rx module (Rx_MD) includes the following basic functional components:

- The receiver electronic photonic integrated circuit (Rx_EPIC) which comprises two channels with each channel comprising:
  - 1 Polarization beam splitter and rotator (for polarization diversity)
  - 2 Delay Interferometers (DI) (for polarization diverse DPSK reception)
  - 2 photo-detectors, (one for each polarization)
  - 1 SiGe BiCMOS transimpedance amplifier with differential output
- One fiber assembly (FA)
- One optical output connector (OC)

3.2 EPIC technology

The modulator and receiver circuits (Tx_ePIC and Rx_ePIC in the functional diagrams above) are designed using IHP SG25H_EPIC technology, a monolithic photonic BiCMOS technology which combines 0.25 µm BiCMOS, high-performance npn HBTs and full photonic device set for C/O-band. The main features offered by this technology are HBTs with f_T/f_{max}=220/290GHz on the electric side and optical waveguides implemented using three available etch depths with a minimum propagation loss of 0.9 dB/cm. Photodiodes with f_{3dB}>60GHz and phase shifters implementing several waveguide doping levels (p, n, p+, n+) are also developed using this technology. The SG25H_EPIC technology is available via IHP MPW service. The figure below shows the cross section of an EPIC mixed substrate. It shows the photonic substrate with a germanium (Ge) photo-diode on the left side and the electronic substrate with a HBT on the right. For the photonic part this substrate is a stack of 750µm bulk Silicon, 2µm Silicon dioxide and 220nm Silicon, while the electronic part substrate is only bulk Silicon.

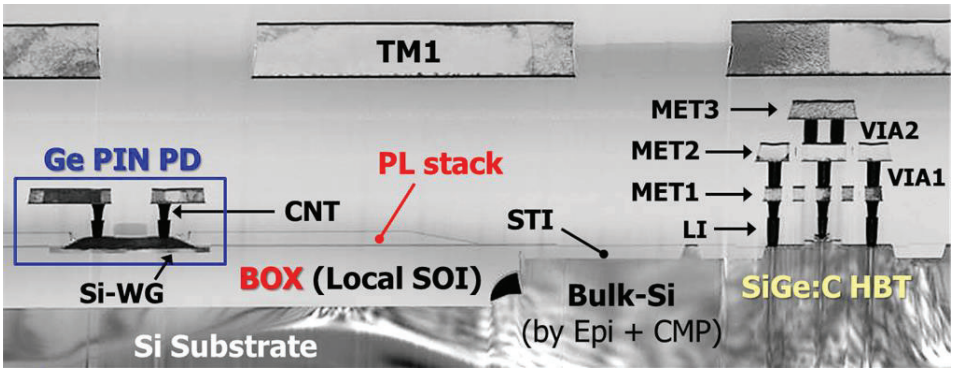

Figure 5: Cross-section of an EPIC's mixed substrate

3.3 Modulator and receiver EPIC

A twin-channel Mach Zehnder Modulator (MZM) / driver was designed and fabricated in IHP SG25EPIC process to realize the Tx-ePIC. The figure below shows the fabricated circuit with layout overlay. The Tx-ePIC hosts >20 opto-

electronic elements (excluding the BiCMOS circuitry) into a chip areas of <15 mm^2. The Tx-ePIC (as well as the Rx-ePIC) is equipped with inverse taper spot size converters for edge coupling.

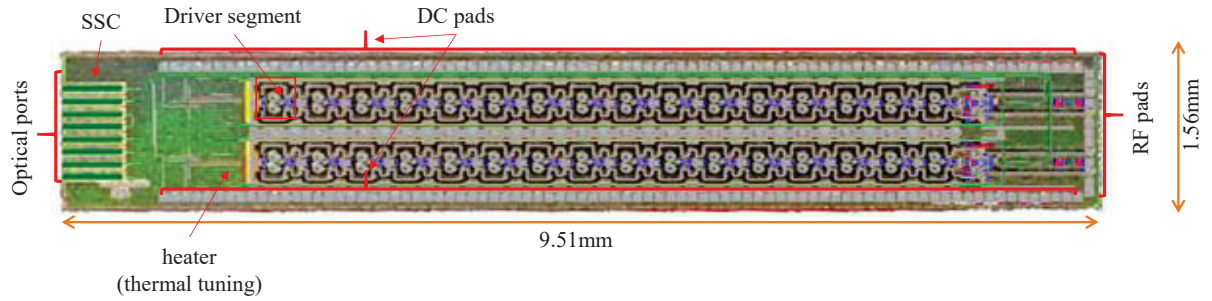

Figure 6: Fabricated Tx-EPIC with layout overlay.

The MZM operates via the plasma dispersion effect and relies on carrier depletion to realize electrical modulations of free carriers within the silicon waveguide. The MZM is designed as a dual-drive segmented (SE-MZM) structure and comprises a number of phase shifter segments driven by a segmented driver distributed along the phase shifter. The SE-MZM approach is chosen in order to maximize the extinction ratio (ER) – here the target is to achieve an ER of 10 dB.

The chip further features the following:

- Optical interfaces placed on the side opposite to the RF interfaces
- Optical couplers at the input and output of the device for signal splitting and combination in the MZM structure
- A straight waveguide section and bend that routes the optical input to the input coupler of the MZM
- Thermal tuning sections placed before the output coupler of the MZM for the operation point adjustment

The opto-electronic performance estimated by layout simulations is as follows:

- Vπ*L = 2.9 V*cm
- ER = 11 dB
- RF output swing (differential) at the modulator 4 V
- RF input swing (differential) ranges from 300mV - 800mV
- Differential input impedance 100 Ω (GSSG configuration)
- Heater resistance: 100 Ohm - Tuning power: 26 mW / pi
- Power consumption per channel = 1.6 W

The table below shows the break down of the EPIC insertion loss (IL) which is estimated to be ~11 dB.

Table 2 Tx-EPIC IL breakdown

Component	**Typical loss range**	**Aggregate typical loss on chip (worst case)**
Spot size converter (6µm MFD)	1 – 1.5	3
Straight waveguide	2 dB / cm	1.2
Splitter / coupler	0.3 – 0.5 dB	1
Phase shifter	1 dB / mm	6
TOTAL loss	-	**11.2**

A twin-channel receiver EPIC (Rx-ePIC) was designed and fabricated in the same process. The figure below shows the fabricated circuit with layout overlay. The Rx-ePIC hosts >20 opto-electronic elements (excluding the BiCMOS circuitry) into a chip areas of <5 mm^2.

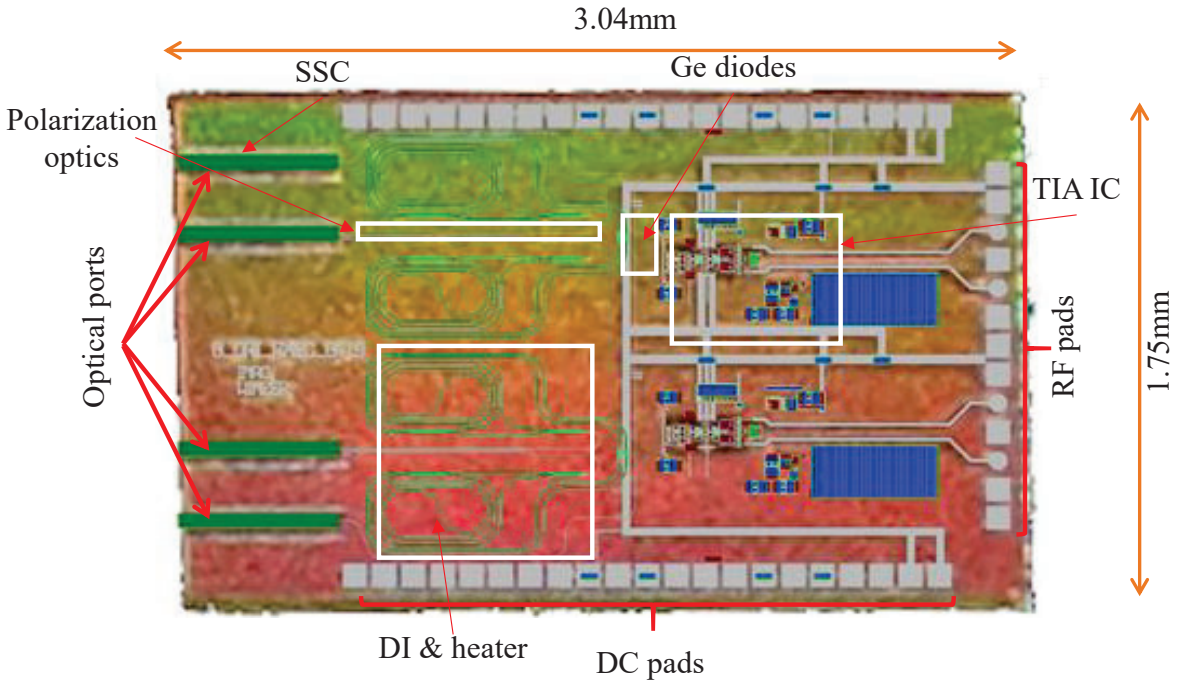

Figure 7: Fabricated Rx-ePIC with layout overlay.

The Rx-ePIC photonic front-end comprises a dual polarization input with integrated polarization splitter and rotator (PSR) and twin delayed interferometers (DIs) for polarization diversity. The DI differential delay is set to 40 ps to match the data rate of 25 Gb/s and is fine-tuned through on-chip heater elements. A pair of Ge diodes waveguide coupled to the DIs is included for photodetection. The outputs of the photodiodes is connected to the transimpedance (TIA) circuit which is used to convert the small input currents from the photodiodes into a differential output voltage. A cascaded 3-stage amplifier circuit provides the amplified differential output RF signal. The photo-generated current from the detectors is converted to voltage by the input stage (VGA1) and amplified to a sufficient voltage swing by the gain stage (VGA2). The output buffer enables to drive external differential 100-Ω load. The figure below shows the block diagram of the Rx-ePIC electronics.

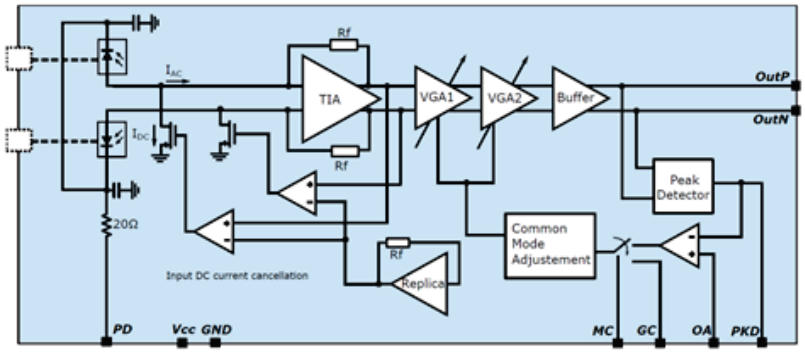

Figure 8: Block diagram of the Rx-ePIC electronics block

As shown in the block diagram, the circuit also features:

- PD bias voltage is externally provided at PD pin and fed to the PD via on-chip low-pass filter
- A peak detector circuit that detects the output voltage
- Common mode adjustment circuit that drives the input and gain stages of the amplifier in manual or automatic gain control mode
- DC-cancellation loop to eliminate the DC offset induced from the single-ended input stage.

The table below shows the break-down of the EPIC insertion loss (IL) which is estimated to be ~3.7 dB. The power consumption per channel is estimated to be 260 mW.

Table 3 Rx-EPIC IL breakdown

Component	Typical loss range	Aggregate typical loss on chip (worst case)
Spot size converter (6µm MFD – measured)	1 – 1.5	1.5
Waveguide section (straight wg and pol. Optics)	0.5 - 1	1
DLI (inc. in/out coupler)	0.8 – 1.2 dB	1.2
TOTAL loss	-	**3.7**

3.4 Transmitter optical sub-assembly design

A transmitter optical sub-assembly (TOSA) design was developed with the aim to define the scheme and process for co-packaging the Tx-ePIC with a DFB LD and enable a compact Tx_MD device. Optical coupling relies on a free-space optical system employed to couple the light from the DFB into the EPIC. In order to incorporate the free space optics elements as well as the multi-channel fiber output, an optical fan-out is included to expand the small pitch of the EPIC waveguide interfaces. Therefore, the input optical path includes the following elements: DFB LD, free space optics, optical fan-out and EPIC. Likewise, a fiber array with standard fiber connectors will be coupled to the output channels through the optical fan-out and the output optical path includes the following: EPIC, optical fan-out and fiber array.

The figure below shows the TOSA CAD model outlining the position and interconnection of the above mentioned photonic elements. The optical fan-out is a Waveguide Array to Fiber Transposer (WAFT) element. The WAFT is a glass PIC manufactured by ion-exchange process, that offers the possibility of full customization of the port count, output pitch and mode sizes over a wide range.

A custom WAFT has been designed in collaboration with a commercial supplier in order to match with the optical interface of the EPIC in terms of pitch (127 µm) and mode field diameter (>3 um).

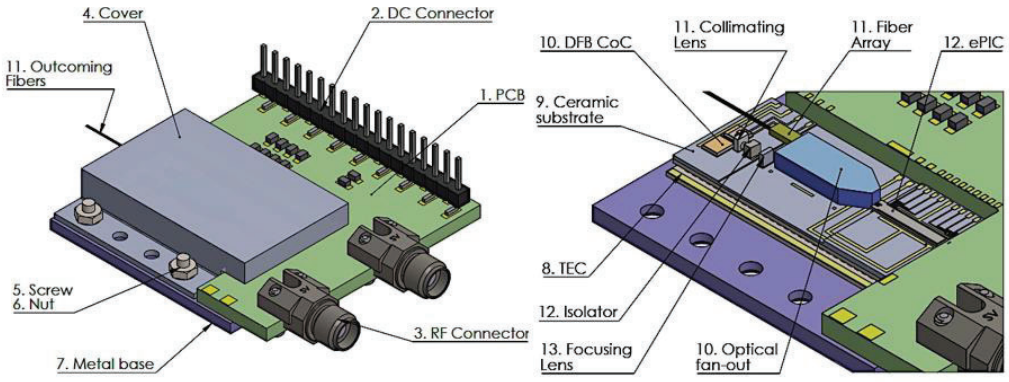

Figure 9: CAD model of the TOSA

The MFD of all the five channels at the fan-out output side is ~10 μm for efficient coupling to a standard single mode fiber. The fan-out has been provided pre-assembled with a 4 channel fiber array. It includes two standard single mode fibers (SMF-28) corresponding to the auxiliary channels, and two PM fibers (SM15-PS-U25A-H) corresponding to the EPIC output channels, all channels being terminated with FC/APC connectors. The insertion losses of the fan-out are ≤0.7 dB for the non-fibered channels and ≤1.2 dB for the fibered channels. The optical path between DFB and WAFT consists of two micro square lenses and an optical isolator, so as to avoid possible noise in the DFB caused by back-reflections. The figure below shows the layout of the simulated free space optical path. The shape of the lenses surface has been designed after simulations with the well-known commercial software ZEMAX considering the numerical aperture (NA) of the DFB and of the interposer waveguide. The nominal coupling loss of the optical system is estimated at 1.42 dB. TOSA assembly and integration is in progress at the time of submission.

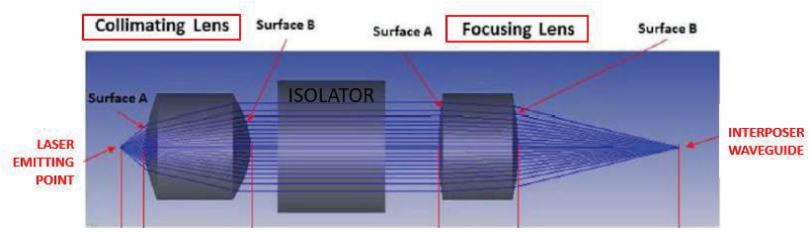

Figure 10: Input optical system layout.

4. CONCLUSION

We have presented the progress of H2020-SPACE-ORIONAS project in the application of new generation laser modems for OISLs. We have presented the physical layer architecture and the development of miniaturized monolithic integrated transceiver circuits. The transceiver chipset reported here features a twin 25 Gb/s DPSK modulator/driver and receiver photonic integrated circuits. Each circuit accommodates two channels (aggregate data rate of 50 Gb/s) and hosts >20 opto-electronic elements into chip areas of <15 mm^2 (modulator) and about 5 mm^2 (receiver) respectively. The aggregate power consumption per channel for the chipset is <2W. Finally we reported the detailed design of TOSA assembly including the definition of the critical optical interfaces between EPIC, laser and fiber assembly.

5. ACKNOWLEDGEMENT

The ORIONAS project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 822002.

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