Design-Driven Metrology: a new paradigm for DFM-enabled process characterization and control: extensibility and limitations.

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ABSTRACT

After more than 2 years of development, Design-Driven Metrology (DDM) is now being introduced into production flows for semiconductor manufacturing, with initial applications targeted at 65 nm and below, but also backward-compatible to 90 nm and above nodes. This paper presents the fundamental components of the DDM framework, and the characteristic architectural relationships among these elements. The discussion includes current status and future prospects for this new metrology paradigm, which represents the true enabler for Design For Manufacturability (DFM) flows and applications. At the core of Design-Driven Metrology lies the simple but powerful concept of utilizing physical design layouts, and more specifically (X,Y) coordinates and polygonal shapes, to automate the generation of metrology jobs. Derived from 10 year old practices of Optical Proximity Correction, the adoption of CAD tools for visualization and manipulation of design layouts, in everyday lithography work, has provided the essential infrastructure for metrology automation. The in-depth discussion of data-flow and system architecture is followed by a presentation of key DDM applications, with specific emphasis on CDSEM metrology, ranging from process development and yield optimization to circuit design. The study concludes with an analysis of the extendibility of DDM and derived flows to other metrology areas in semiconductor manufacturing.

Keywords: Design-Driven Metrology, Design Based Metrology, Metrology Automation, Resolution Enhancement Techniques, Optical Proximity Correction, Design For Manufacturing

1. Introduction

Since its first introduction[1] in 1962 by the philosopher of science Thomas Kuhn, the term "paradigm-shift" has been used (and often abused) to describe a fundamental transition from a consolidated set of perspectives and methodologies towards a superseding new system, which does not simply replace the old one, but rather re-interprets it into a superior and more general framework. It seems therefore appropriate to define the technological framework of Design-Driven Metrology (DDM) or Design-Based Metrology (DBM), as it is often referred to, a true paradigm-shift in the practices of semiconductor design, process control and fabrication.
After more than 2 years of development DDM is now being introduced into production flows, with initial applications targeted at the 65 nm node and below, but also backward-compatible to 90 nm and above nodes. At the core of DDM lies the simple but powerful concept of utilizing physical design layouts, and more specifically (X,Y) coordinates and polygonal shapes, to automate the generation of metrology jobs.

1.1. A very brief history of RET and OPC

In order to understand how and why DDM has reached the stage of maturity at this particular point in the integration roadmap, it is necessary to examine from a historical perspective, the introduction and development in the last ten years of Resolution Enhancement Techniques (RET) and Optical Proximity Correction (OPC) in lithography.
It is well known (and it has been described in detail in the technical literature[2,3,4,5]) that the continuing success of lithography in supporting Moore's Law is due to the synergy of RET, which allows for patterning to occur in the sub-wavelength domain and its complement OPC, which allows for the RET induced distortions (optical and process proximity effects) to be reduced and mitigated, thus restoring a manufacturable process window.
OPC was first implemented in the form of Rule-Based OPC (RB-OPC) around the 180 nm node as table driven sets of rules, specifying edge movements (corrections) for given distances (proximity) between polygonal shapes in a layout.

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Between the 130 nm and the 90 nm node this ever-growing table of correction rules was replaced by an empirically calibrated full-chip fast process simulator. In Model-Based OPC (MB-OPC) an iterative algorithm tries to minimize the difference between a predicted and a target edge through a sequence of simulation and edge movement steps.
An essential (and sometimes overlooked) element of the RET/OPC flow is its software integration within the layout physical verification environment and specifically into the Design Rule Check engine. Since MB-OPC does not necessarily converge to a zero error (target edge vs. simulated edge) for a general layout, an additional computational step of post-OPC verification is needed in order to classify the residual errors and allow for a disposition mechanism to be established. This last step, which is termed Layout Printability Verification (LPV) for sake of generality in this study, (and which includes the various commercial designations of ORC, LRC, MRC, SiVL, etc.) is critical for production OPC at 65, 45 nm and below. Thus the complete patterning solution is determined when lithographic tool, process, RET, OPC and LPV components are specified.
This short historical survey highlights the fact that the use of full-chip physical layouts is now completely embedded into day-to-day lithographic practices, both during technology development and in production. DDM was therefore conceived as a natural evolution from OPC practices, but its impact extends well beyond OPC and even lithography as it will be discussed in the following sections.

1.2. From Layout Printability Verification to Design-Driven Metrology

The catalyst for the implementation of a DDM production flow was provided by the need to experimentally validate LPV checks. For instance typical LPV checks might include “Minimum Line-Width Violation” “Minimum Space-Width Violation”, etc. and such violations could be flagged because of either a real patterning problem or sometimes because of an incorrect algorithmic coding of the rule, or a too stringent numerical specification, or a classification error, or in general some other LPV predictive power limitations. From a metrology perspective, experimental validation for LPV check is analogous to OPC model calibration, but with a potentially much higher number of required measurements. Furthermore while measurement for OPC models can be in principle collected without specifying the exact locations of OPC test structures on the wafer, as long as the necessary “types” of measurements are collected, LPV validation most often requires a measurements at an exact location on the layout and corresponding location on wafer, especially for unique or near-unique 2-dimensional patterns. Without a DDM flow the only possibility is manual navigation on the metrology tool, searching and hunting around the silicon wafer for a large number of patterns: an impractical approach undermining RET/OPC verification, and creating a costly bottleneck in the design to fabrication chain.

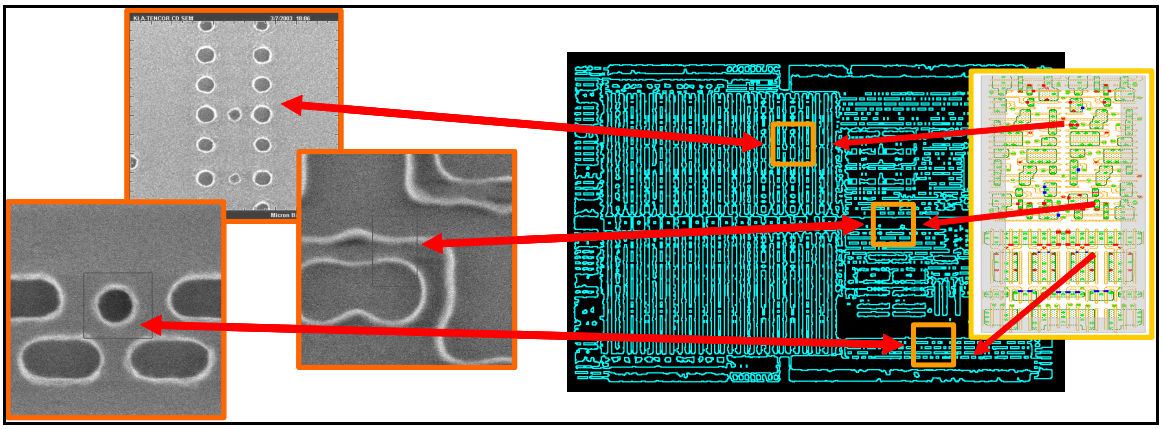

Figure 1: From Layout Printability Verification to Design-Driven Metrology

This study will illustrate how the LPV validation problem has been solved in the most general way (Figure 1), giving rise to Design-Driven Metrology flows and applications and ultimately creating a fundamental “enabler” for the burgeoning field of Design For Manufacturing (DFM). Following a detailed description of the overall DDM flow and the architectural software components of the system, selected applications, both in the design front-end and in the

silicon fabrication back-end will be presented, to exemplify the general applicability of this innovative metrology framework. Finally, DDM extensions beyond CD-SEM, current limitations and future developments will also be discussed.

2. Design Driven Metrology: Data-Flow and Architecture

2.1. DDM Data-Flow

The physical design layout (Figure 1.a) is the obvious starting point in the DDM data-flow. Typically, for a VLSI integrated device (either product or test-chip) several **layout components** are assembled together. Without loss of generality, in this study, the terms layout and layout component will be used interchangeably. Also, in the general DDM framework layout components will be assumed to contain polygonal data for various drawn layers, target layers, (post-OPC) masking layers, and verification (both geometric and simulation based) layers in the fabrication process, plus additional optional design annotation data.

A **metrology site-list** (MSL) is then extracted from a given layout component. A MSL can be described as a structured (strongly-typed) spreadsheet, with a variable number of columns. A minimal set of columns includes a unique identifier for a metrology site, corresponding (X,Y) coordinates and units, and region of interest information. Additional columns might include metrology algorithm type, geometric proximity data, layout references, etc. Physical implementations of MSL range from simple ASCII-text spreadsheets to richer and more structured XML syntax.

The extraction operation of a MSL represents the computational abstraction of a very large set of complex selection algorithms, which need not to be specified in the DDM flow. As it will be shown in the later section on advanced DDM

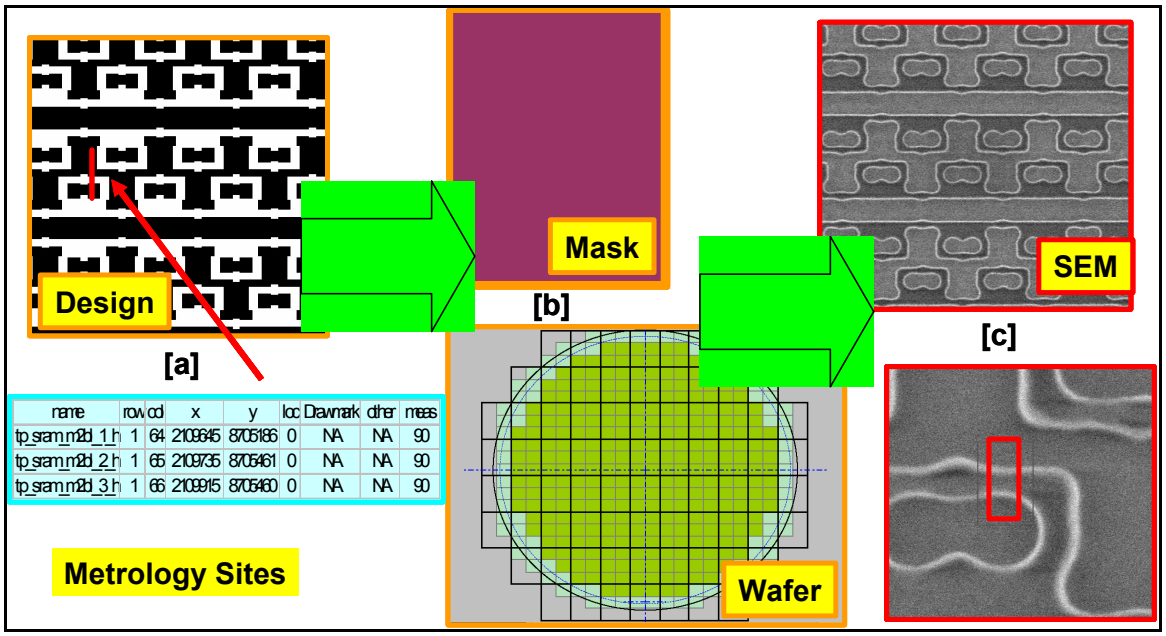

Figure 2: Design Driven Metrology Flow

applications, MSL can be generated manually by "point-and-click" selections in a layout browser, or by heuristic filtering of post-OPC verification checks or even from electrical analysis of critical circuits. The creation of MSL is not limited to applications in the design space, but can also be the result of one metrology step being linked to another metrology step. For instance defect inspection could provide a MSL for a CD-SEM tool or a MSL for mask metrology could be also passed to any type of wafer metrology. Thus the combination of a layout component and related MSL defines the fundamental interface for the DDM data-flow.

Two families of geometric coordinate transformations (Figure 2.b) are then needed to link layout components and their MSL with corresponding locations of actual integrated devices on silicon wafers. The first set of transformation defines the mask (or reticle) through placement of all required layout components. A layout component can be magnified, rotated and mirrored during placement. Additionally a layout component can be placed multiple times (arrayed) onto a mask.
The second set of transformations, from mask to wafer, involves the selection of portions of the reticle to be imaged and the placement of these *mask-images* into rectangular arrays of dies (wafer-maps), in order to maximize the printable silicon area and optimize yield. Again the geometric operations involved are magnification, rotation, mirror and array.
The final step in the DDM data-flow (Figure 2.c) consists of the definition of a general interface to the (vendor) specific metrology tool. In addition to the layout components and related MSL, mask selections and wafer selection must be passed downstream. It is important to observe that because of the two array operations included in the transformations from layout to mask and from mask to wafer, the total number of metrology sites, which are passed downstream in the DDM flow, is given by the cardinality of the MSL times the selection of sub-dies in the mask and the selection of dies on the wafer. For instance if a MSL contains 15 metrology sites and 2 sub-dies out of 4 in the mask are selected for measurement, and 10 dies out of 200 are selected on the wafer, the total number of measurements will be 300.
Again comprehensive metrology selections data (including all transformations, explicit and/or implicit) can be assembled in a structured file (preferably XML syntax) and merged with tool specific (static) data. Performance (file-size) considerations might require that only clipped portions of the original layout components are provided to the software metrology interface. The use of clipped layouts is now the current practice in production DDM implementations. Thus polygonal data (clipped or full layouts) and complete metrology selections (including design to mask to wafer transformations) provide the most general interface for all type of DDM applications.

2.2. DDM Software Architecture

A number of software implementations can be mapped onto the previously described DDM data-flow. Within the scope of this study it is important to describe only the 3 different architectural domains implicit in DDM (Figure 3).
In the first domain (Figure 3.a) a variety of EDA software applications extract MSL from layouts. As it has been mentioned before, these MSL extractors might be based on: process development, yield optimization, OPC verification, critical circuit analysis, etc. Because of the generality and the flexibility of the DDM paradigm any, software application which outputs a spreadsheet of coordinates from a layout can be used in a DDM flow. Detailed examples will be covered in the next section.

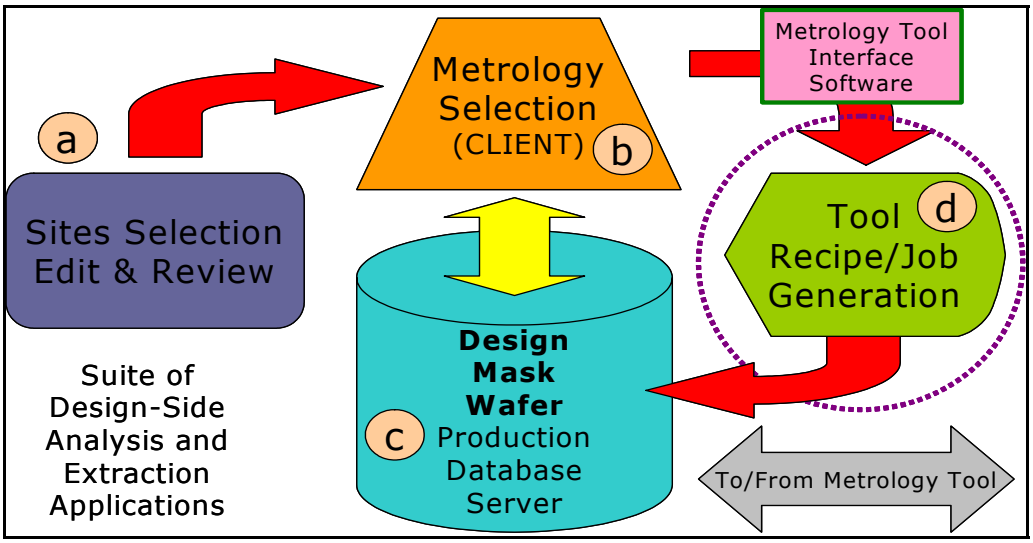

Figure 3: DDM Software System Architecture

The second software domain (Figure 3.b, 3.c), which will be denoted as Design-Mask-Wafer (DMW) database, represents the true enabler of DDM. The DMW, as the name implies, contains all transformations necessary to map any coordinate from the design space onto any coordinate in the mask space and then onto corresponding coordinates in the wafer space. Notice that these relational mappings are 1 to many and many to many.
In the forward portion of the DDM flow the basic application built on top of DMW consists of the metrology mask sub-die selection and the wafer die selection. In the feed-back portion of the DDM flow metrology results are uploaded to the database repository for further analysis.
In the current state-of-the art in semiconductor manufacturing, only custom proprietary implementations of DMW exist. The generality of the DDM framework allows for DMW to support both vertically integrated semiconductor manufacturing and foundry production models, while the interface to the first DDM software domain (EDA space) allows for fabless design operations to be augmented with a powerful, but previously impractical, metrology flow.
Finally the third software domain (Figure 3.d) is composed of an increasing number of vendor specific metrology software applications, which provide the direct interface to the metrology tool. These applications automate the creation of the metrology recipe (job), thus improving productivity and accuracy.
Interfaces to CD-SEM metrology have been the first DDM components to be implemented and are now reaching post-beta maturity, entering production at 65 nm. Although it is obvious that each metrology tool (beyond CD-SEM) which is inserted in a DDM flow requires a custom software interface, nevertheless the software elements in the DDM CD-SEM interface include a prototypical set of functionalities common to all DDM tool interfaces (current and future). The next section describes these essential components and the architectural relationships among them.

2.3. Design-Driven CD-SEM Metrology Interface

Various Design-Driven software applications exist, which automate SEM recipe generation. For sake of generality in this study, the term Metrology Tool Interface (MTI) will be used to denote such applications (Figure 4). The term can be extended to other metrology tools such as inspection, overlay, etc.

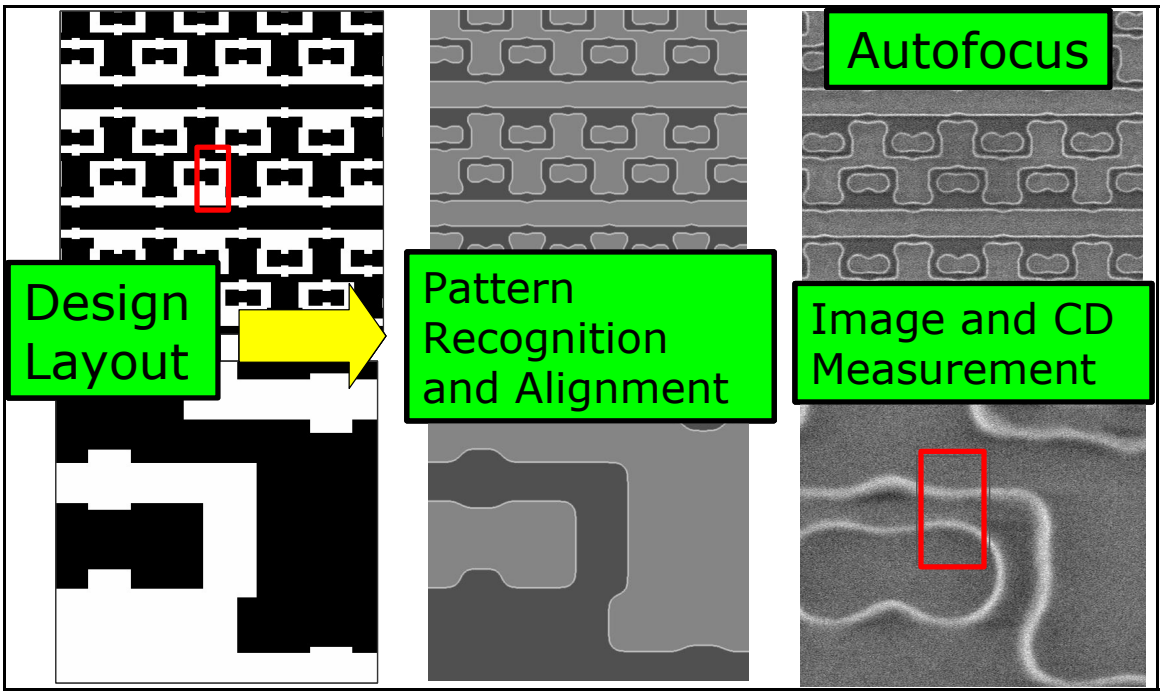

Figure 4: Metrology Tool Interface Flow for DDM

While vendor-specific syntax might vary for a MTI, inputs necessarily includes polygonal data in the form of layout components (most often layout clips) and metrology site selections (including implicit or explicit mapping of design

coordinates onto mask and wafer spaces). Additional information about reference coordinates, global alignment, metrology algorithms, and tool settings are also provided.
For every metrology site, polygonal data for the surrounding region (region-of-interest or ROI plus a larger peripheral geometric context) is used to drive local pattern recognition and alignment (PRA). Advanced algorithms for robust pattern recognition constitute the foundation of a MTI application.
In general layout polygonal data, which are essentially binary bitmap images, cannot be used directly for PRA, but must be processed to resemble images of real patterns on silicon as they are acquired by the microscope. This means that suitable image processing algorithms must be used to include both (a) lithographic processing effects and (b) electron beam scanning image acquisition effects (including forward and backward scattering, charging due to different substrates, conductive and dielectric layers interactions and pattern morphology). Speed performance trade-offs don't allow rigorous modeling and simulation of either (a) or (b). Some MTI implementations include some sort of lithographic simulation, which might prove more predictive, especially for process-window test wafers (Focus-Exposure Matrix) at the expense of pattern recognition speed and overall recipe generation time (not to mention the additional input-data requirement on lithographic process conditions). Other MTI implementations use heuristic-based image emulation, with sophisticated dynamic range gray-scale adjustments and contrast balancing, in order to optimize PRA accuracy and recipe generation time.
A minimally acceptable PRA success-rate for a production-worthy MTI is at least 95%, with 98% and 99% production targets. Development of advanced PRA algorithms is a continuing activity and no standard production targets have been defined at this time for total SEM recipe generation times. This second figure of merit (recipe generation time), which might vary from less than a hour to few hours depending on the number of sites, wafer processing conditions and geometrical characteristics of the patterned shapes is less critical than PRA success-rate, as long as recipe generation can be performed on a MTI computer hardware *independent* of the SEM tool. Detailed state-of-the art results can be found in the technical literature[6,7].
Selection of the optimal area for automated focus setup (autofocus) is another critical component of a MTI. Again geometric layout data (possibly from multiple layout layers) is used for this operation. Specific layout information is integrated with a selection of already optimized tool-specific and process step-specific recipe settings (often referred to as Best-Known-Methods or BKM) which are dynamically selected (using heuristic algorithms in the MTI) during recipe generation.
Finally the MTI must also provide the core functionality for image acquisition and measurement (Figure 5). The selection of the most suitable (rectangular) region to image is an intrinsically difficult problem, strongly dependent on the type of site to be measured and its pattern topology. Thus different algorithms are required for lines and spaces, for line-ends, for various 2D features, for circular versus elongated contacts, etc. Currently available MTI provide an extensible library for these advanced image measurement algorithms[8].

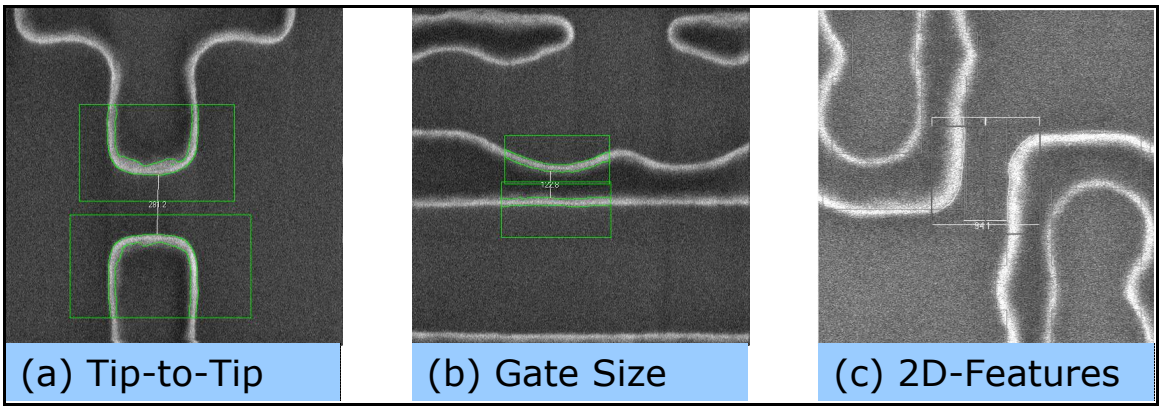

Figure 5: Image Acquisition and Automated Measurement Box Placement

A special mention must be given to the measurement sites clustering problem (Figure 6.a). An advanced MTI is characterized by the presence of an algorithmic functionality for determining a single image acquisition region for a cluster of specified metrology sites, in order to optimize the execution of the SEM job and at the same time reduce charging effects. Depending on the specific measurement implementation (after image acquisition) this problem can be

solved using various strategies. The most efficient strategy, in order to optimize SEM job speed and throughput, consists of acquiring high resolution SEM images and then perform all (clustered and un-clustered) measurements in a post-processing mode. Another strategy relies on in-line (i.e. on the SEM) metrology algorithms in order to improve measurement accuracy.
Whether in-line or post-processing, new advanced measurements algorithms are being developed at an accelerated pace, because of the catalytic effect of the DDM framework.

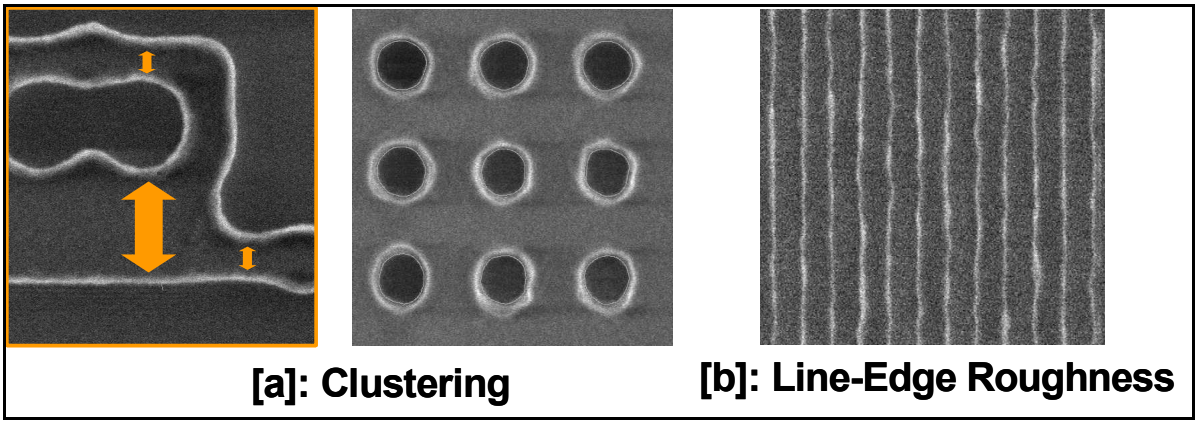

Figure 6: Advanced Measurement Algorithms

In addition to pure image processing algorithms like extraction of Line Edge Roughness (LER) (Figure (6.b), the availability of layout shapes allows for novel algorithms to be implemented, among which, most notably, direct determination of measured Edge Placement Errors (EPE)[9], i.e. differences between patterned edges and design-target edges (Figure 7). The combination of accurate alignment with respect to an absolute reference (when available) in the layout together with image processing for contour extraction, allows also for the determination of asymmetric EPE, another important OPC calibration and verification figure of merit.

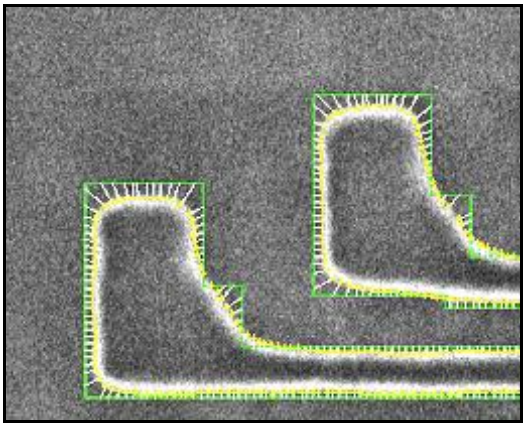

Figure 7: Automated Extraction of Edge Placement Errors
(Image courtesy of Cyrus Tabery, AMD, H. Morokuma, Hitachi High-Technologies Corp.)

Other MTI are being developed in analogy with the CD-SEM interface. Wafer inspection MTI and overlay MTI are two examples. In both cases the implemented software functions must support parsing and analysis of layout data (across several layers) and coordinate mapping, as previously described. Differently from CD-SEM applications, MTI for inspection and overlay must include image processing algorithms dependent on the specific metrology. For instance a variety of optical simulations (pre-processing) can be included in the overlay MTI, while noise reduction rules in defect detection, based on pattern densities, can be implemented in the inspection MTI.

3. Advanced DDM Applications

3.1. OPC Model Generation

The creation of increasingly accurate and predictive OPC models has been one of the main drivers for the development of the DDM framework. The construction of a typical OPC model requires two distinct experimental data sets: (a) the calibration metrology set and (b) the verification metrology set. The first group of measurements is used for the actual model fitting (calibration), while the predictability characterization of the calibrated model is performed using the second group of measurements. Extraction of MSL for both (a) and (b) is a routinely automated task in OPC development, whose output feeds directly into the DDM interface. An additional benefit of DDM consists of the possibility of utilizing locations inside product dies (and not limited to test structure in scribe lines) for predictability verification, thus improving the overall quality of the OPC model (Figure 8).

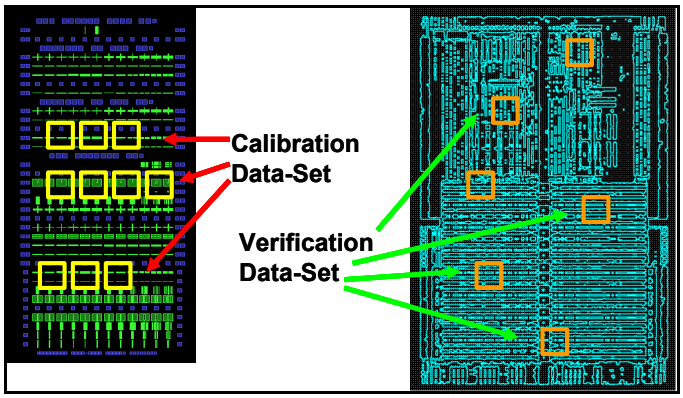

Figure 8: Advanced OPC Model Generation using DDM

3.2. Design Rules Selection and Optimization

Adoption of Layout Printability Verification methodologies in the selection and optimization of Design Rules (DR) for a new technology node, stems directly from the non-linear effects introduced by the RET, as it has been described in the introductory section of this study.

A systematic approach for evaluating candidate DR sets for a given technology begins with the identification of "classes" of Design Rules. For instance, as shown in Figure 9, there are several types of a "Corner Bend Distance" rule and similarly several types of a "Minimum Line-End Distance" rule.

Each type of rule is then represented as a Parametric Test Pattern (PTP), where the rule is fully specified by the values of a number of geometric parameters, as in Figure 10.a. Each PTP is implemented as a programmable layout generator, capable of synthesizing thousands of test patterns, based on a table of ranges for the PTP parameters. The complete layout becomes part of a full Design-Of-Experiments (DOE) where DR variants, RET selections and different OPC algorithms can be assessed in an integrated fashion to determine an acceptable design space (Figure 10.b).

During the experimental validation portion of this methodology the DDM framework is utilized to select and measure locations for candidate DR. It is important to observe that such a systematic flow can only be implemented because of the availability of DDM, given the very large number of experimental data point which must be collected.

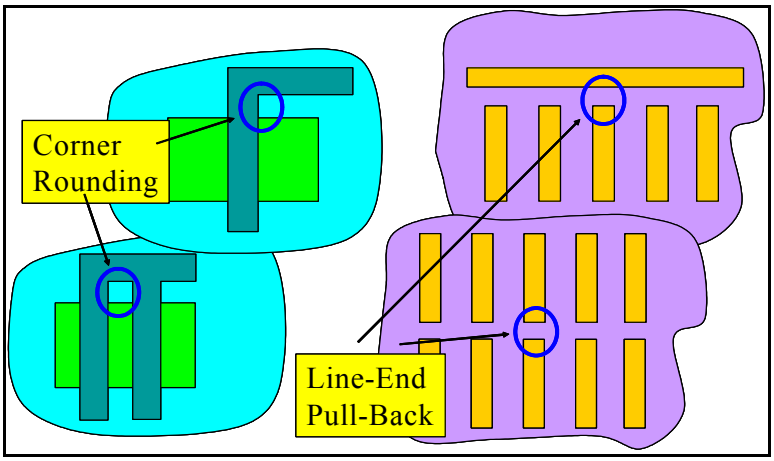

Figure 9: Classes of Design Rules

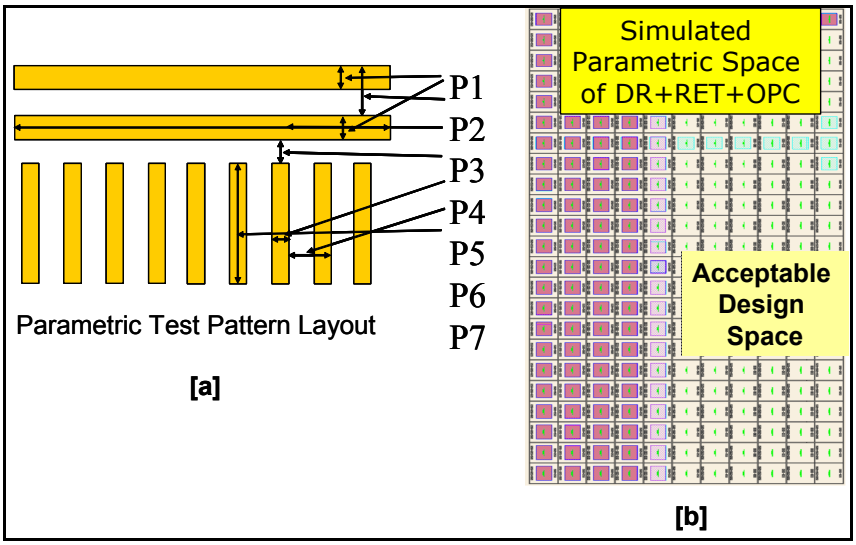

Figure 10: Parametric Test Pattern and DOE Simulation for DR Optimization

3.3. Si-based Timing Analysis and Non-Rectangular Transistor Modeling

These two applications in the circuit design domain illustrate power and versatility of the DDM framework, well outside the traditional process development and wafer production spaces. In both examples a novel flow for extracting MSL from circuit design data is coupled with the universal, straightforward DDM flow.

The first application consists of the generation of a MSL from transistor gates locations in selected critical speed-paths, for an advanced microprocessor. As it was presented[10,11] in 2005 timing extraction with post-OPC simulated gates results in a re-ordering of the criticality of several speed-paths and in the additional discovery of new critical speed-paths (Figure 11.a).

Again DDM enables circuit designers to request targeted CD-SEM measurements on the exact transistors for the specified critical paths, to be correlated with traditional parametric electrical testing.

In the second application, aimed at the characterization and modeling of non-rectangular transistors[12], MSL are again built from specified gates, but also along the longitudinal width of each gate as well. DDM allows for a precise specification of the measurement location directly correlated with circuital components (Figure 11.b).

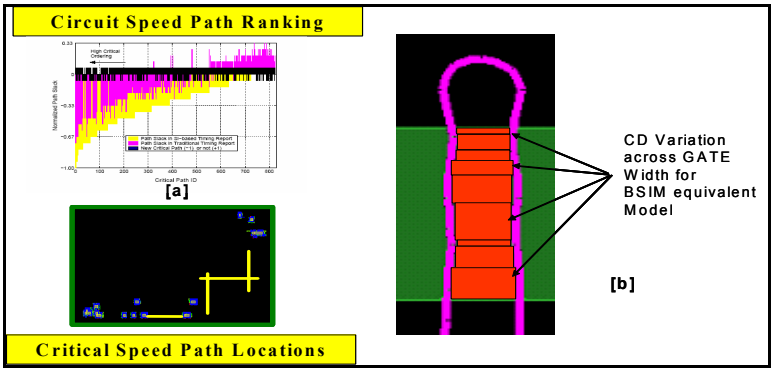

Figure 11: Circuit Design Applications for DDM

3.4. Pattern-Matching of SEM Images on Layouts

In this final DDM application, locations for a MSL are extracted using a novel flow based on 2D ultra-fast, image based pattern matching software[13]. The pattern matcher can identify not only all "exact" occurrences of a given polygonal clip (provided as a bitmap image) in a full-chip layout, but also, with a decreasing "match-factor" several occurrences of "geometrically similar" shapes (fuzzy-matching).

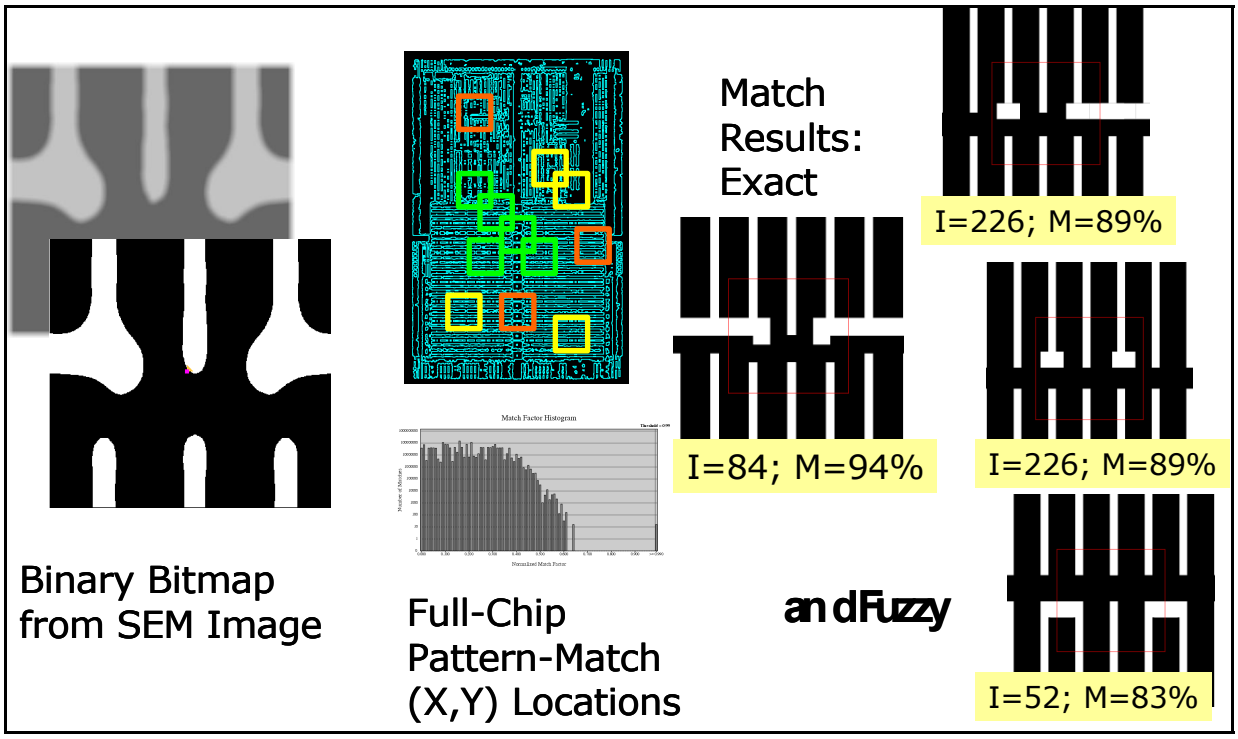

Figure 12: Pattern matching of SEM Images on a Full-Chip Layout

Often in FAB environment, when a potential yield detractor is identified, it is necessary to validate the corresponding CDSEM measurement (and image) using other locations across the die with the same patterned shape, in order to verify systematic and/or random characteristics of the suspect yield problem.

From the initial single SEM image a complete series of metrology locations (MSL) can be generated by first converting the SEM image into a binary bitmap (through conventional edge detection algorithms) and then performing a pattern-matching analysis on the full-chip layout. The results, as shown in Figure 12, include locations of the exact original patterns and also locations of geometrically similar layout shapes which can be used for further validation and disposition of the yield detractor. In this advanced application the DDM flow is used in a "feedback" mode, where initial locations spawn further (extended and refined) metrology selections.

4. Future developments and conclusions

The DDM framework has been fully implemented for SEM metrology and it is entering production at 65 nm and 45 nm, with backwards compatibility in 90 nm and above. DDM is also extensible to other metrology tools, wherever physical design layout data can be used to drive, control and support the automated creation of metrology jobs and recipes, and corresponding analyses of results. Extensions to Wafer Inspection and Overlay metrology have been discussed in the previous sections.

Process Control (APC/APM) is also a potential development area for DDM. While the use of full-chip layout data is clearly too cumbersome for real-time process-control applications, off-line (a-priori) layout analysis can drive hierarchical strategies and heuristics for "optimally escalated" APC data acquisition.

This study has illustrated the role of DDM as the fundamental enabler of Design For Manufacturing, linking the now pervasive use of layout data in semiconductor FABS with "upstream" applications in the design domain. An ever growing number of applications are predicated on the "universal' DDM interface.

DDM also allows for yield characterization and optimization by directly using product design information, in addition to traditional test-chip based methodologies. This capability will be essential at 45, 32 and 22 nm technology nodes.

The original DDM framework was deployed in a vertically integrated device manufacturing environment. Architecture flexibility allows for extensions to foundry-fabless models, provided that a suitable collaborative platform between metrology tool equipment vendors and EDA software suppliers can also be developed.

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