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Abstract. We present a prototype electron emitter array integrated with an active-matrix driving large-scale integrated circuit (LSI) for a high-speed massively parallel direct-write electron-beam (e-beam) system. In addition, we describe the results of a performance evaluation of it as an electron source for massively parallel operations. The electron source is a nanocrystalline Si (nc-Si) ballistic surface electron emitter in which a 1:1 projection of the e-beam can resolve patterns 30 nm wide. The electron-emitting part of the device consists of an array of nc-Si dots fabricated on an SOI or Si substrate and through silicon via (TSV) plugs connected to the dots from the back of the substrate. The device consists of an aligned joint of TSV plugs with driving pads on the active-matrix LSI. Electron emissions are driven by the LSI and are boosted to an appropriate level using a built-in voltage level shifter in accordance with a bitmap image preliminarily stored in the embedded memory. Electron emissions from a test array work as intended, showing the possibility of switching on and off the beamlets by changing the CMOS-compatible voltage. © 2012 Society of Photo-Optical Instrumentation Engineers (SPIE). [DOI: 10.1117/1.JMM.11.3.031406]

1 Introduction

Nanoscale lithographic technologies have been intensely studied for the next generation of semiconductor manufacturing. Maskless/direct-write electron-beam (e-beam) lithography is a candidate for the upcoming 16-nm node and beyond. It compares well with projection technologies such as a combination of 193 nm immersion lithography and self-aligned spacer double patterning and/or extreme ultraviolet (EUV) lithography. At present, however, a direct-write e-beam system remains challenging as far as achieving an acceptable throughput for mass production goes; i.e., a throughput improvement of more than three orders of magnitude will be required for commercial semiconductor/micro electro mechanical system (MEMS) fabrication. Massive parallelism has been suggested as a potential way around this roadblock,[1] and many innovative concepts in multiple e-beam imaging have been proposed and are being developed.[2–8] If a commercial level of throughput can be achieved, this technology can potentially reduce the cost of manufacturing photomasks for the next generation of ultra-large-scale integrated circuit (ULSI) devices, as well. In addition, it could enable a timely response for making diversified photomasks for MEMS devices made in high-mix, low-volume production.

These potential industrial advantages prompted us to begin development of a massively parallel direct-write e-beam system with a throughput comparable to that of existing optical steppers. The expected throughput using a system described in Sec. 2.1 could be 10 to 100 wafers (300 mm in diameter) per hour, depending on the switching speed, data transfer rate, and electron beam current density. The electron source used in this system is a nanocrystalline Si (nc-Si) ballistic surface electron emitter,[9,10] in which a 1:1 projection of the electron beam can resolve patterns 30 nm in width.[11] An array of microminiaturized nc-Si electron emitters are integrated with an active-matrix driving large-scale integrated circuit (LSI), and the beamlets exposing pixels in parallel are operated at a CMOS-compatible voltage. This paper presents our prototype nc-Si electron emitter array compatible with the active-matrix driving LSI, and it discusses an experimental evaluation of the performance of an electron source for massively parallel exposure.

2 Basic Concept of the System

2.1 System Configuration

The whole system embodies an array of microcolumns, each having an nc-Si electron emitter array in combination with microminiaturized electron optical elements for projecting a reduced image (1/100) of focused e-beams. The

microcolumns have very small physical dimensions, and they are made by utilizing MEMS fabrication technology. The result is a compact overall mechanical system with substantial cost benefits. Figure 1 shows the configuration of the miniaturized column consisting of the active matrix nc-Si electron emitter array, an array of condenser lenses, anode plates, a rotation coil, telecentric reduction lenses, deflectors, and collection optics providing functions of dynamic focusing, alignment collection, and deceleration. Also embedded are metrology systems, i.e., a stigmator for astigmatism correction and a Faraday cup for real-time monitoring of the projected pixel images.

The nc-Si emitters are arranged in a $1,000 \times 1,000$ pixels array with a pitch size of 10 μm. The array covers an area of 10×10 mm^2 and is integrated with the active-matrix driving LSI. The one million beamlets projecting pixels simultaneously are switched on and off by changing the CMOS-compatible voltage. The constitutive array of condenser lenses consists of a grid of electrostatic Einzel-type lenslets, which collimate the emitted electron beams from the emitter. The array of lenslets is separately fabricated and mechanically bonded onto the array of nc-Si emitters (see Fig. 1). The bonding process is currently under development in which each is aligned in a one-to-one manner with the required accuracy of a submicrometer by using a piezo-actuated manipulator under in-situ scanning electron microscope (SEM) observation of the fabricated alignment marks. Fabrication of monolithically integrated lenslets with the array of nc-Si emitters are also being studied in parallel. The nc-Si emitter exhibits favorable emission properties in terms of its perpendicularity (i.e., lower emission angle) and uniformity over the whole surface,[12] originating from the ballistic transfer of electrons passing through the nano-silicon-wired-array structures. This feature allows the condenser lenses to be easily designed so as to collimate and focus the emitted electrons, leading to reduced beam size

(1/10) and increased current density ($\times$100) for each electron beam without any change in pitch size (10 μm). Each of the electron beamlets passing through the array of condenser lenses is accelerated at the anode plate through apertures with an acceleration voltage of $\sim$20 keV. The beamlets then enter a telecentric reduction lenses consisting of two electromagnetic lenses. Here, they are focused to project a reduced image onto the wafer. The two embedded deflectors scan the focused beamlets to perform the direct-write operation in synchronization with the controlled motion of the stage.

2.2 Compensation of Chromatic and Spherical Aberrations

Since a general rotationally symmetric lens system cannot make a concave lens creating a negative aberration, neither chromatic nor spherical aberration can be compensated by optimizing the configuration of the electric and magnetic fields in the electron optics presented in Fig. 1. Chromatic aberration is inherently generated by the energy dispersion of the emitted electrons, and this restricts the practical resolution of the system. Our previous study demonstrates that the initial energy dispersion of emitted electrons from an nc-Si ballistic emitter is innately small (approximately 2 eV at RT and 500 meV at 100 K),[11,13,14] and thus, the chromatic aberration can be sufficiently optimized by making the energy distribution as close to monochromatic as possible. In this regard, we are improving the physical properties of nc-Si itself, as well as exploring other potential schemes such as operating the emitter at a lower temperature, which has been demonstrated to significantly reduce energy spread of the emitted electrons.[11,13,14] On the other hand, spherical aberration should be compensated on a reduced image projected by the telecentric reduction lens system in order to improve the practical resolution. It can be corrected by controlling each of the driving voltages in the picture cells of the integrated LSI, so that the spatial distribution
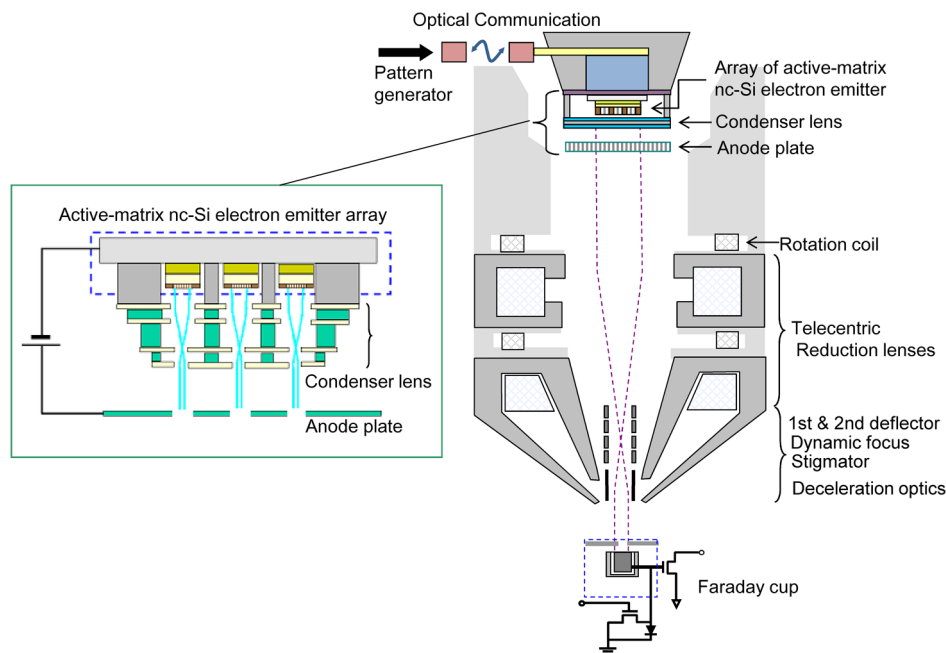

Fig. 1 Configuration of the miniaturized column having an active-matrix nc-Si electron emitter array in combination with microminiaturized electron optical elements.

of the emitted beamlets' energy can be adjusted to compensate for the spherical aberration and be balanced on the projected image. At present, we are studying how to incorporate such a function into the next design of the LSI.

3 Prototype of Nanocrystalline Silicon Emitter Array

3.1 Evaluation of Emission Characteristics from Prototype Dot Pattern Array of nc-Si Emitters

The active-matrix electron emitter includes an array of nc-Si dot patterns, each connected electrically to through silicon via (TSV) plugs from the back side of the supportive substrate. The device consists of an aligned joint of the TSV plugs with driving pads on the active-matrix LSI. In prototyping this device, a test structure was preliminary fabricated to ascertain if the electron emissions from the array would work in practice; a 2-μm-thick nondoped columnar polycrystalline silicon (poly-Si) film was deposited on a 4-inch n^+-type Si substrate, and the poly-Si was dry-etched with a photoresist mask to form an array of 100×100 dots with a pitch of 50 μm, each dot having an area of 20×20 μm^2. After that, a 0.15-μm-thick Si$_3$N$_4$ film was deposited over the whole wafer surface by low-pressure chemical vapor deposition (LPCVD). Then, apertures were opened on the Si$_3$N$_4$ film with a photoresist mask at the top surfaces of the dots by highly selective reactive-ion-etching (RIE) of the Si$_3$N$_4$ film over the underlying poly-Si layer in a mixture of CHF$_3$/CF$_4$ gas. After the individual poly-Si top surfaces were exposed, each was selectively anodized in a HF solution, which promoted preferential local dissolution at the poly-Si grain boundaries and resulted in structured porous silicon. Because of the columnar geometry of the poly-Si grains, the fabricated porous silicon includes nanodots with columnar/vertically arranged interconnections similar to nanometric wires ("nanowires").

The anodization was conducted as follows: The processed 4-inch wafer was diced into 12 pieces; each specimen measured 20×20 mm^2 and was grooved into a working electrode of a Teflon sample holder in contact with the backside surface. This was followed by mechanical screw-clamping of the top surface to seal the back surface from the solution (see Fig. 2). An anodic current was galvanostatically applied for 6 s to the working electrode in a solution of HF (55%): C$_2$H$_5$OH = 1:1 at a current density of 25 mA/cm^2 under the irradiation of a tungsten lamp.
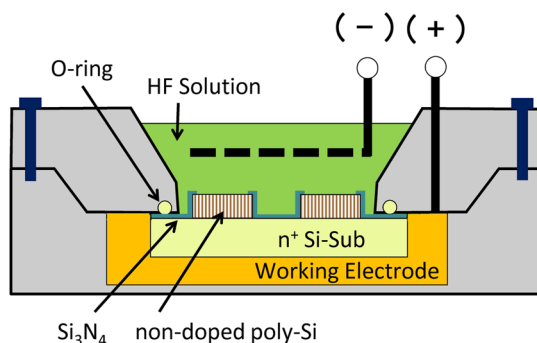

Fig. 2 Electrochemical etching of patterned poly-Si for structuring a Si nanowire array.

After that, the sample was treated with rapid-thermal-oxidation (RTO) at 900°C in a dry O$_2$ ambient for 25 min to form a thin oxide layer surrounding each Si nanodot in the nanowire array. The surface was then treated with high pressure water vapor annealing (HWA) at 1.3 MPa and 260°C for 3 h and subsequent super critical rinse and dry (SCRD) in order to obtain sufficiently passivated nc-Si/SiO$_2$ interfaces. The interfaces had an extremely low defect density, because of the minimized mechanical stress of the surrounding SiO$_2$.[15] Then, a Cr/Au (=300 nm) common electrode was selectively RF-sputtered by using a liftoff process with resist mask onto an area excluding the top surfaces of the dots. This was followed by depositing a Ti/Au (=1 nm/9 nm) surface electrode over the whole surface. This two-step deposition process improves step coverage for each dot pattern, even for extremely thin surface electrodes. Figure 3(a) shows an SEM image of the fabricated test structure array consisting of a 100×100 dots pattern of nc-Si emitters. The corresponding structure is schematically illustrated in Fig. 3(b).

Figure 4(a) shows the characteristics of the diode current density J_{ps} and corresponding emission current density J_e as a function of applied voltage V_{ps} obtained from the sample shown in Fig. 3. The measurement circuit is displayed in the upper part of the figure. The J_e plot shows electron emissions from the emitter array at >4.5 V exceeding the work function of the Au electrode. The current density reached 10 μA/cm^2 at 15 V, which corresponds to an amplified electron current density of 1 mA/cm^2 passing through the integrated condenser lenslets ($\times$100) (see Fig. 1). Figure 4(b) is a Fowler-Nordheim (FN) plot obtained from the emission curve in Fig. 4(a). It should be noted that the linear behavior covered the whole range of applied voltage, although the emission exhibited variability in the low voltage region (<10 V), presumably due to a space charge effect of the emitted electrons with relatively low kinetic energy. The linearity of the FN plot suggests that electrons were ballistically transported via cascade tunneling through interconnected nanodots in the silicon nanowires.

3.2 Fabrication of nc-Si Emitter Array on SOI Substrate for Integration with the Active-Matrix Driving LSI

nc-Si emitters were fabricated on SOI substrate with via-last processed TSV plugs connected to the array from the back side, with each plug and emitter forming an aligned joint with driving pads on the active-matrix LSI.

The essential features of the fabrication process are illustrated in Fig. 5. As shown in this figure, a 2-μm-thick nondoped columnar poly-Si film is deposited on a 4-inch SOI wafer having an n^{++}-type active layer (0.005 Ωcm). The active layer/poly-Si stacking structure with a photoresist mask is dry etched, until the underlying active layer on the BOX is 50 nm thick. The resulting array of 100×100 dots covers an area of 20×20 μm^2 (steps 1-2). Next, CF$_4$/CHF$_3$ RIE is used to conduct a highly selective sidewall-spacer etching of 0.15-μm-thick LP-CVD Si$_3$N$_4$ over the underlying active layer (step 3). After the wafer is diced into smaller specimens, these smaller specimens are anodized in a HF solution with the electrochemical cell shown in Fig. 2. Immediately after that, they are treated with RTO + HWA + SCRD under the same conditions described in Sec. 3.1
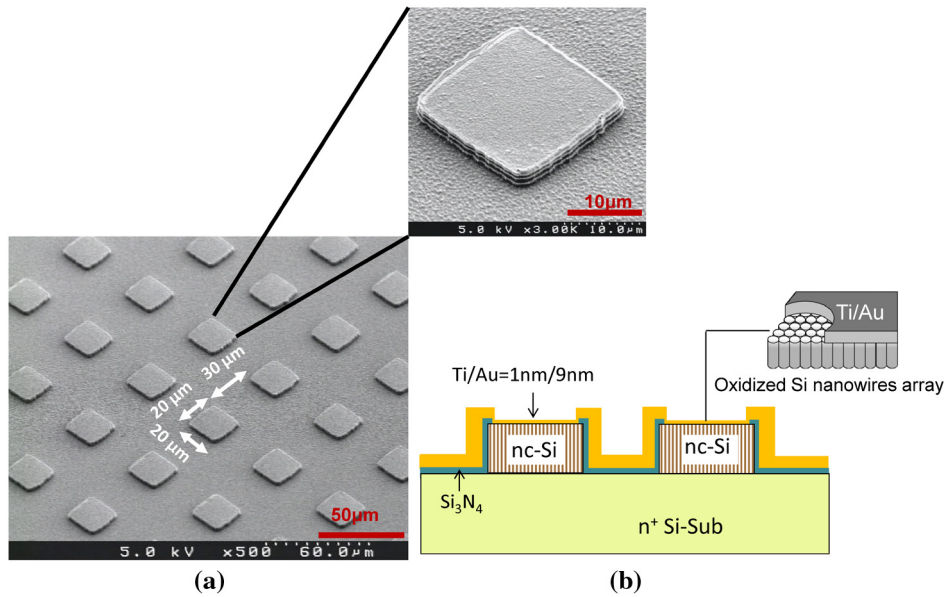
Fig. 3 (a) SEM image of the fabricated test structure of a 100×100 array of nc-Si emitters with a pitch of 50 μm, with each emitter having an area of 20×20 μm^2; (b) schematic illustration of the corresponding structure.
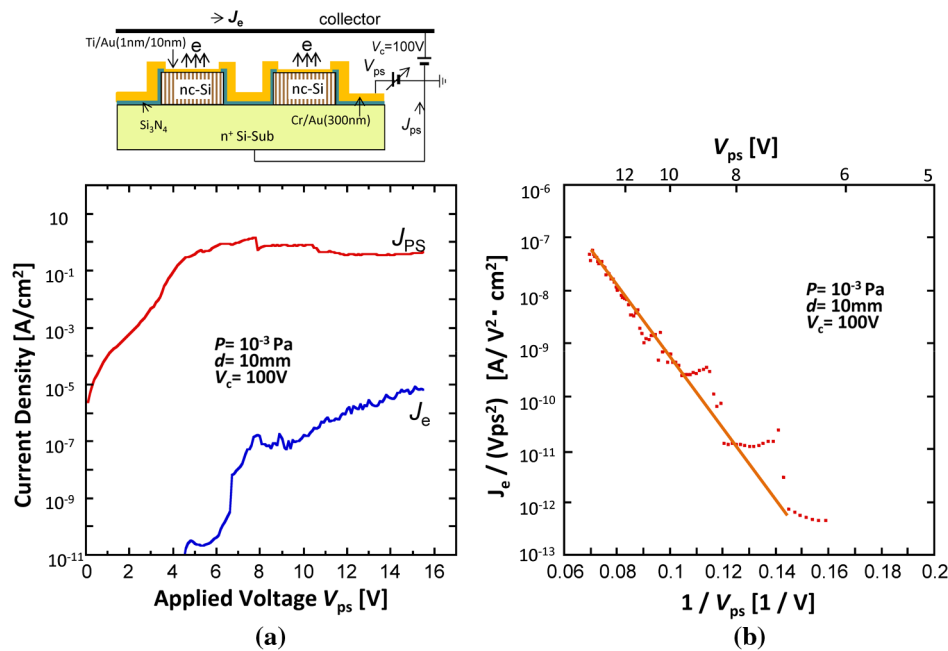

Fig. 4 (a) Characteristics of diode current density J_{ps} and corresponding emission current density J_e vs. applied voltage V_{ps}; (b) Fowler-Nordheim plot obtained from Fig. 4(a).

(step 4). Then, Ti/Cu via-filled TSV plugs (steps 5 to 6), solder bonds with the active-matrix LSI through the Au–Sn bump structures (step 7), and electrodes (step 8) are formed.

Galvanostatically anodizing the structure fabricated on an SOI substrate (step 4) leads to an extremely high potential due to the difficulty of injecting carriers through the BOX layer if the working electrode is connected only to the back of the sample. In fact, the potential reached several tens of volts when an anodic current was applied under the galvanostatic condition of 25 mA/cm^2; such a situation is probably accompanied by an undesirable BOX breakdown

process. Thus, during the anodization process in step 4, the working electrode was connected directly to the top surface, bypassing the remaining n^{++} active layer in the upper part of the surrounding sidewall of the grooved substrate. The remaining n^{++} active layer among the dots was dissolved and became porous and easily oxidized to form an insulating layer in the subsequent RTO treatment. This layer formed a self-aligned electrical separation among the dots, resulting in complete separation of the pixels.

Nanostructures constituting the nc-Si cause the band gap to widen due to the quantum confinement effect.[16] Experimentally exposing a YAG Laser (266 nm) on an anodized
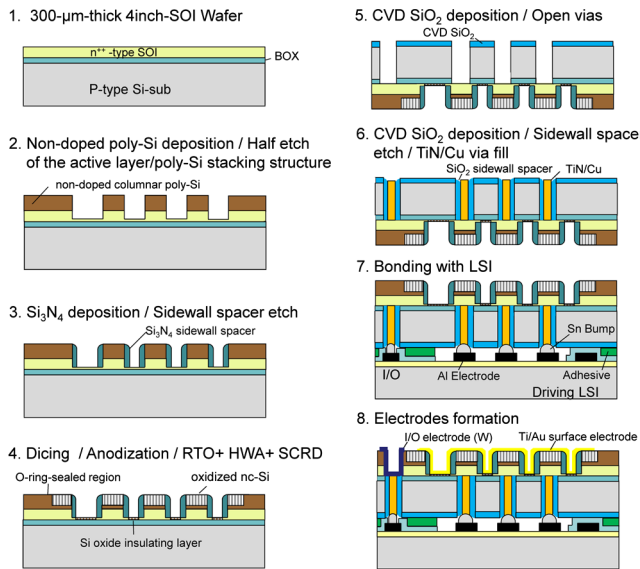
1. 300-μm-thick 4inch-SOI Wafer

2. Non-doped poly-Si deposition / Half etch of the active layer/poly-Si stacking structure

3. Si₃N₄ deposition / Sidewall spacer etch

4. Dicing / Anodization / RTO+ HWA+ SCRD

5. CVD SiO₂ deposition / Open vias

6. CVD SiO₂ deposition / Sidewall spacer etch / TiN/Cu via fill

7. Bonding with LSI

8. Electrodes formation

Fig. 5 Schematic illustration of the fabrication process flow of an nc-Si emitter array integrated with active-matrix driving LSI. The nc-Si emitter array was fabricated on SOI substrate with via-last processed TSV plugs.

poly-Si surface on SOI substrate with subsequent RTO + HWA treatments under the same conditions as described in step 4 led to red band photoluminescence (PL) with a peak intensity at a wavelength of ~700 nm (1.8 eV) (see Fig. 6). This indicates that Si nanowire array structures with a derived size of ~3 nm were formed.[16] Electron emissions were also observed from this sample through a subsequently deposited Ti/Au (=1 nm/9 nm) electrode on the top surface in association with applied
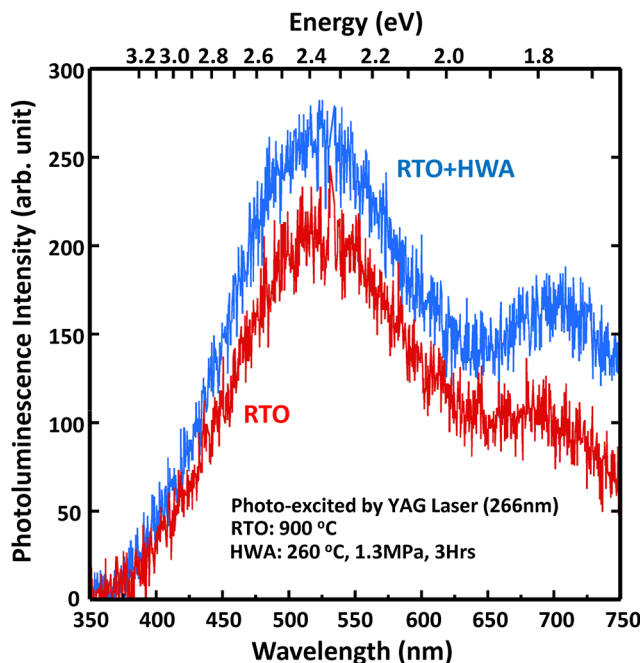

Fig. 6 Photoluminescence (PL) spectra obtained from anodized non-doped ply-Si surfaces on SOI substrate with subsequent treatments of RTO and RTO + HWA.

voltage, demonstrating that the anodizing process is workable on an SOI substrate, as well as on Si.

Figure 7(a) shows an SEM image of the structure just after step 4 in Fig. 5. The corresponding structure is schematically illustrated in Fig. 7(b). The anodizing process in step 4 could be conducted at a lower applied anodic-voltage (~3 V) for galvanizing the 25 mA/cm². As shown in Fig. 7(a), a 100 × 100 array of nc-Si emitters with a pitch of 50 μm, each having an area of 20 × 20 μm², was successfully formed on the SOI substrate. Cross-sectional SEM observation showed that the layer remaining among the dot patterns was sufficiently oxidized as an insulating layer, and the thickness was approximately 50 nm over the whole surface.

3.3 Advanced Fabrication Process for nc-Si Emitter Array

The results described in Secs 3.1 and 3.2 demonstrated that the array of 100 × 100 microminiaturized nc-Si emitters worked in practice by emitting ballistic electrons and was manufacturable on an SOI substrate, thereby enabling us to integrate it with an active-matrix driving LSI. However, the fabrication process shown in Fig. 5 remains a challenge for processing larger wafers for mass production in terms of SOI usage related to cost benefit, as well as the manufacturability of the anodization process. Figure 8 shows an advanced structure and corresponding fabrication process flow to address these issues. Here, the nc-Si emitter array is fabricated on a Si substrate with via-first processed TSV plugs filled with an n^{++}-type LP-CVD poly-Si film. All of the processes are done on 4-inch Si wafer, and they can be extended to larger wafer processes. Since most of the processes shown in Fig. 8 include many of the processes described in the previous section, only the essential features will be described here.

A 200-μm-thick 4-inch Si wafer (p-type, 5k Ωcm) is deep-reactive-ion-etched (Deep-RIE) with a photoresist mask to open through-silicon-vias (15 μm in diameter) with a pitch of 50 μm, and a thermally grown SiO₂ layer is formed over the whole surface (steps 1-2). Next, an n^{++}-type LP-CVD poly-Si film is deposited over the whole surface to completely fill the vias, and both surfaces are chemical-mechanical polished (CMP) until the remaining n^{++}-poly-Si thickness on one surface is thinner (~2 μm) than the thickness on the other surface (step 3). After that, a 2-μm-thick nondoped columnar poly-Si film is deposited on the thinner side, and a 200 × 200 array of dots with a pitch of 50 μm (each dot having an area of 20 × 20 μm²) is formed on the n^{++}-poly-Si/nondoped poly-Si stack structure (step 4). Next, thermally grown SiO₂ film and LP-CVD Si₃N₄ film are deposited and patterned on the top surfaces of the dots (step 5). Subsequently, each exposed poly-Si surface is anodized by galvanostatically applying an anodic current from the back of the n^{++}-poly-Si film (step 6). After RTO + HWA + SCRD treatment, the back side n^{++}-poly-Si is patterned as an electrode, and an aligned joint with driving pads is formed on the active-matrix LSI through Au-Si eutectic bonding (step 7). Finally, a Ti/Au surface electrode is formed, and half-cut dicing is done to expose the bonding pads of the LSI (step 8).

This advanced process yields not only cost benefits by using Si substrate instead of SOI, but also increased manufacturability for mass production in the anodization process
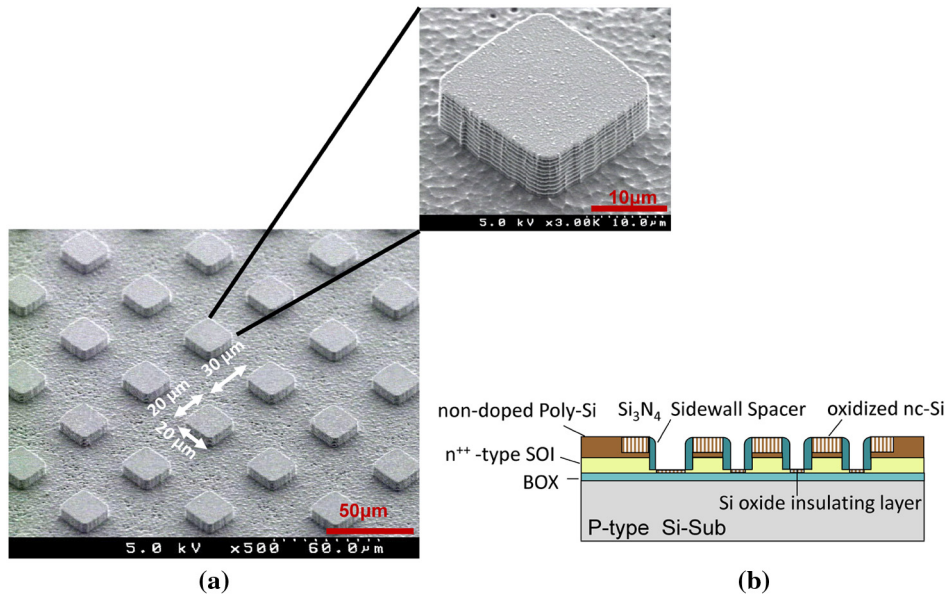
Fig. 7 (a) SEM image of a 100×100 array of nc-Si emitters fabricated on SOI substrate with a pitch of 50 μm, with each emitter having an area of 20×20 μm^2; (b) schematic illustration of the corresponding structure.
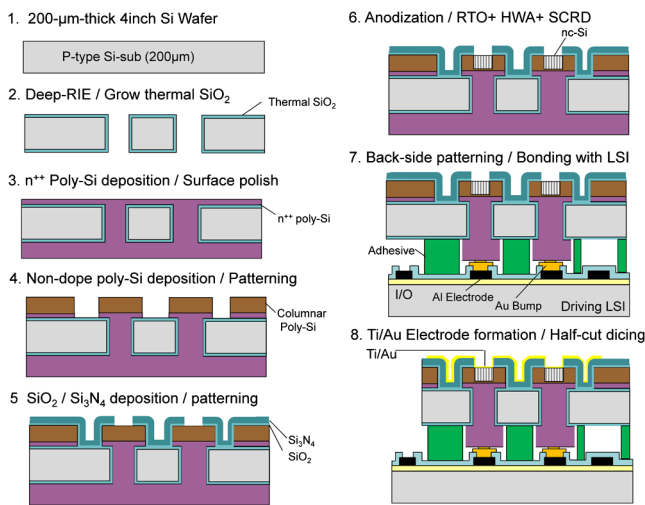

Fig. 8 Schematic illustration of the advanced process flow for fabricating an nc-Si emitter array integrated with active-matrix driving LSI. The nc-Si emitter is fabricated on Si substrate with via-first processed TSV plugs.

by applying a uniform galvanostatic current to each dot from the back of the wafer through each filled via.

4 Design and Prototype of the Active-Matrix Driving LSI

This section presents our first prototype active-matrix LSI circuit, which is capable of simultaneously driving all pixels of the nc-Si electron emitter array in accordance with a bit-map image preliminarily stored in a built-in memory. The bitmap image is temporarily stored and sequentially output in conjunction with input data by switching the driving voltage on and off. The LSI consists of three circuit blocks: a data-line driver circuit, a gate line drive circuit, and a 100×100 bit cell array with a 100-μm pixel pitch, with each cell having a two-bit memory and a driving electrode. The chip size is 12.4×12.4 mm^2, including the largest circuit block of the bit cell array, which is 10×10 mm^2.

Figure 9(a) illustrates the signal operation of the prototype 100×100 active-matrix LSI. The pattern layout of one bit cell is shown in Fig. 9(b). Figure 10 is the timing chart of
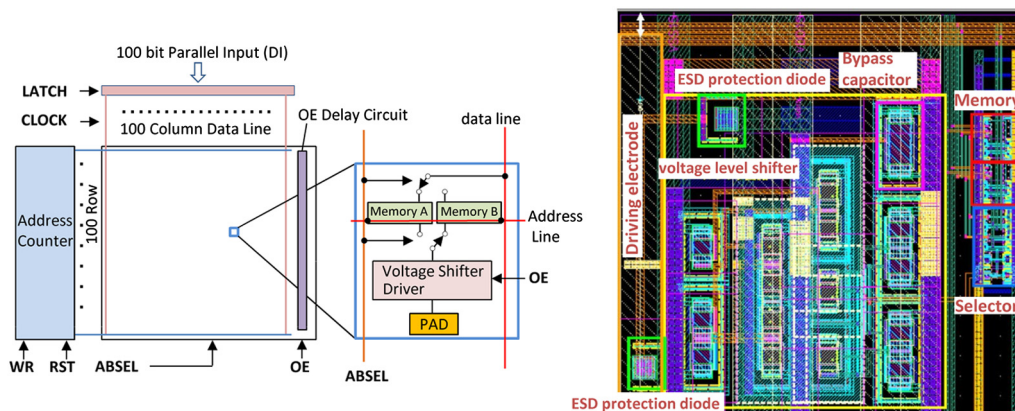

Fig. 9 (a) Signal operation of prototype 100×100 active-matrix driving LSI; (b) pattern design of one cell of the circuit.
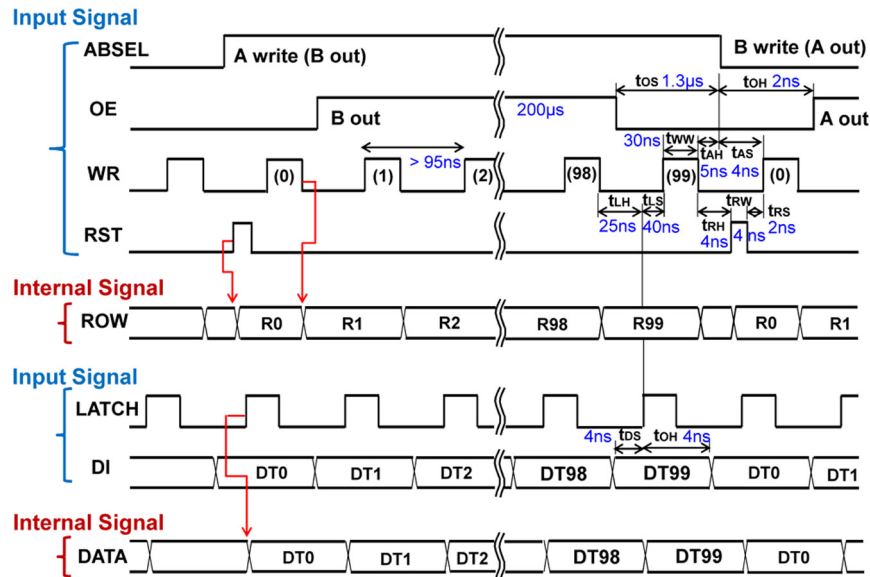
Fig. 10 Timing chart of an active-matrix driving LSI. Each time displayed in the illustration indicates the minimum time of an individual control signal, as calculated by simulation.
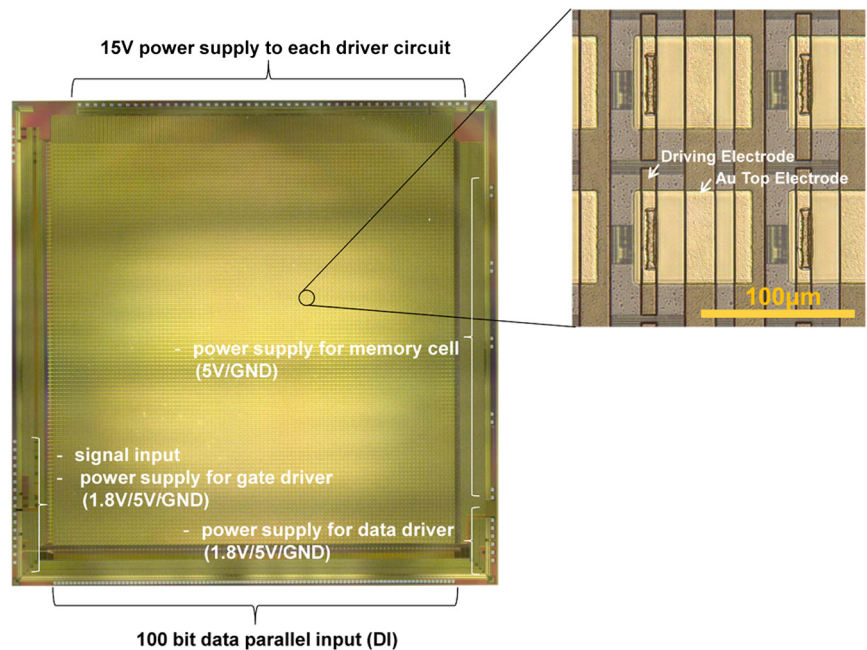

Fig. 11 Optical photomicrograph image of the prototype active-matrix driving LSI circuit.

the circuit, in which the minimum time value of the individual control signal, as confirmed by simulation, is displayed in the figure.

The boldface symbol names (LATCH, CLOCK, WR, RST, ABSEL, OE) in Fig. 9(a) represent input signals (see Fig. 10). DI represents 100-bit data externally input in parallel, which is subsequently latched by the LATCH signal input and stored in a 100-column data line as a set of row data by the data-line driver circuit, as shown in Fig. 9(a). Each row of data (100 bits) is sequentially written by the gate line drive circuit into a selected row address data line during a specific period of time given by ABSEL, RST, and WR signal inputs, resulting in writing of the 100×100

pixels data into each memory of the bit cell array, as shown in Figs. 9(a) and 10. The two-bit memories (A, B) in the one-bit cell shown in Fig. 9(a) enable parallel operations of projecting a bitmap image stored in memory A at the time of the output enable (OE) signal input and writing the next exposure of 100×100 pixels data into memory B. The OE signal input is time delayed on a row address to row address basis by the embedded OE delay circuit, as shown in Fig. 9(a), in order to restrict the peak current passing through the internal circuits. Electron emissions are driven by the LSI applying an output voltage to each bit cell, boosted to the appropriate level by the built-in voltage level shifter.

Figure 11 shows an optical photomicrograph image of the prototype active-matrix driving LSI that we are working on integrating with the nc-Si emitter array described in Fig. 8. In the integration process, the 50-μm pixel pitch of the emitter is to be adjusted in the patterning process of the backside poly-Si electrode (step 7 in Fig. 8), so as to be able to form an aligned joint with this LSI. The integrated device's basic function as an electron source for massively parallel exposure will be tested in order to provide feedback for the next prototype of the device.

5 Conclusions

We described a prototype nc-Si electron emitter array compatible with an active-matrix driving LSI for a massively parallel direct write e-beam system. We conducted a successful experiment showing that ballistic electrons were emitted from an array of 100×100 microminiaturized nc-Si emitters, and that the beamlets could be switched on and off by changing the CMOS-compatible voltage. The nc-Si emitter array was confirmed to be manufacturable on SOI substrates, as well as Si, which allows us to integrate it with the active-matrix driving LSI. Basic functions of the prototype 12.4×12.4 mm^2 active-matrix driving LSI were also confirmed. The LSI has a 100×100 bit cell array with a 100-μm pixel pitch. Each cell has a two-bit memory and a driving electrode. The unit was designed to be able to simultaneously drive all the pixels of the nc-Si electron emitter array in accordance with a bitmap image preliminarily stored in a built-in memory.

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